WA20-5822

Full Digital Audio Amplifier 20Wx2

Rev1.0 – 28 Jun. 2023

1. General description

The WA20-5822 is a single chip full digital audio amplifier including power stage for stereo amplifier system. WA20-5822 is integrated with versatile digital audio signal processing functions, high-performance, high-fidelity fully digital PWM modulator and two high-power full-bridge MOSFET power stages.
The WA20-5822 receives digital serial audio data with sampling frequencies of 32kHz, 44.1kHz, 48kHz, and 96kHz. It delivers 2 x 20 watts in stereo mode without heat sink.
The WA20-5822 has a mixer and Bi-Quad filters which can be used to implement the essential audio signal processing functions such as loudness control, compensation of a loudspeaker response and parametric equalization.
All the functions of the WA20-5822 can be controlled by internal register values via I^2C host interface bus.

2. Features

- 2 CH Stereo (20W x 2 BTL)
- Wide Operating Supply Voltage Range (5V to 26.4V)
- Flexible Audio Interface
  - I^2S / TDM Interface for Audio Input
  - SDATA Generator (I^2S output)
- Floating-Point Operation
- Up to 40 Programmable Bi-Quad Filters
  - Loudness Control
  - Speaker Compensation
  - Parametric Equalizer
- 3 Band Dynamic Range Control
  - Acc (Accelerated) DRC
- Post Signal Processing for Optimized Speaker Control
- Audio Enhancement Algorithm
  - Loudness Compensation
  - Virtual Expander
  - Dynamic Bass
  - Dialog Clarity
- Pre-Scaler and Post-Scaler
- Various Useful Functions
  - Volume and Soft Mute Control
  - Power Meter
  - Smart PWM Switch On / Off
- DC Protection
  - DC-Cut Filter
  - Coefficient Memory Checksum
  - Modulation Index Check
- Protection Circuit
  - OCP (Over Current Protection)
  - OTP (Over Temperature Protection)
  - UVP (Under Voltage Protection)
- High Efficiency (>90%)

3. Applications

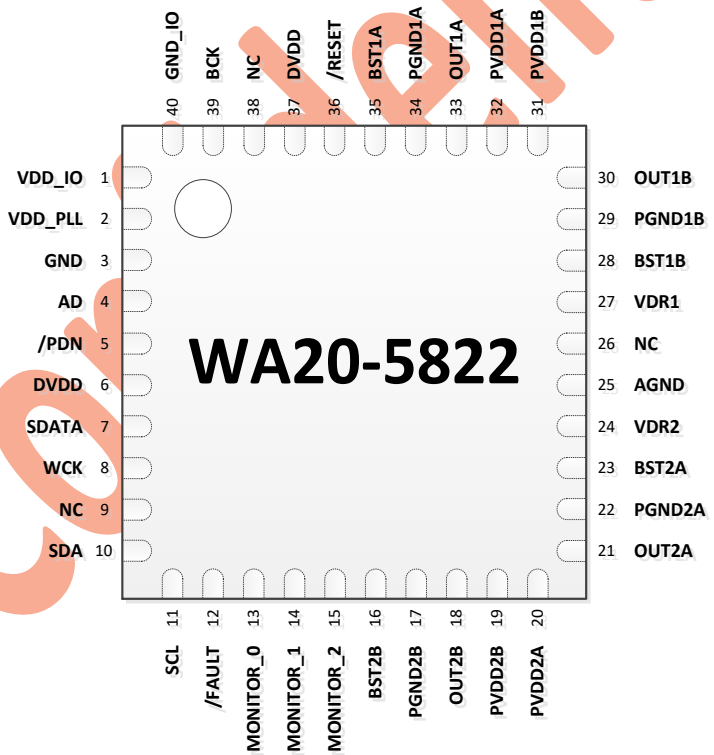
- OLED/UHD/FHD TV or Monitor TV
- Docking Station
- Mini-Component Audio Solution
- Bluetooth Speaker, AI Speaker, Sound Bar

4. Package Information

Type number	Package		
	Name	Description	Marking
WA20-5822	40QFN 6x6	QFN package	WA20-5822

5. Pin Information

Top View



5. Pin Information (Continued)

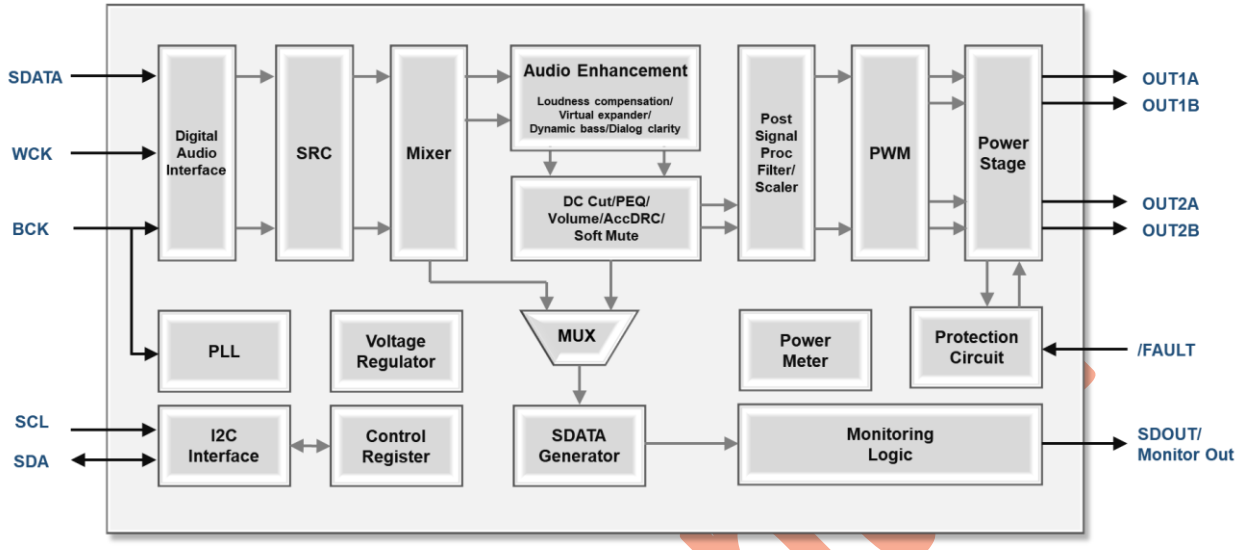
WA20-5822, (40QFN 6x6 Package)

Pin No.	Name	I/O	Function
1	VDD_IO	P	Power supply for digital interface I/O, 3.3V
2	VDD_PLL	P	Regulator output for PLL digital block, 1.2V
3	GND	P	This pin should be connected to Ground
4	AD	I	I^2C device address selection
5	/PDN	I	Power Down
6	DVDD	P	Regulator output for Core block, 1.2V
7	SDATA	I	I^2S serial data input
8	WCK	I	I^2S word clock
9	NC	-	No connection
10	SDA	I/O	I^2C data
11	SCL	I	I^2C clock
12	/FAULT	I	Active low to reset internal power stage, Pull-up
13	MONITOR_0	O	No Connection, monitoring signal out from protection logic
14	MONITOR_1	O	Monitoring signal out from processor / I^2S output (SDATA word) / I^2C slave addr2 <refer to page 13>
15	MONITOR_2	O	Monitoring signal out from processor / I^2S output (SDATA word)
16	BST2B	P	Bootstrap supply, external capacitor to OUT2B is required
17	PGND2B	P	Ground
18	OUT2B	O	Power stage PWM output 2B
19	PVDD2B	P	Power supply for PWM Power stage 2B
20	PVDD2A	P	Power supply for PWM Power stage 2A
21	OUT2A	O	Power stage PWM output 2A
22	PGND2A	P	Ground
23	BST2A	P	Bootstrap supply, external capacitor to OUT2A is required
24	VDR2	O	Gate drive voltage regulator output, capacitor to GND is required
25	AGND	P	Ground
26	NC	-	No connection
27	VDR1	O	Gate drive voltage regulator output, capacitor to GND is required
28	BST1B	P	Bootstrap supply, external capacitor to OUT1B is required
29	PGND1B	P	Ground
30	OUT1B	O	Power stage PWM output 1B
31	PVDD1B	P	Power supply for PWM Power stage 1B
32	PVDD1A	P	Power supply for PWM Power stage 1A
33	OUT1A	O	Power stage PWM output 1A
34	PGND1A	P	Ground
35	BST1A	P	Bootstrap supply, external capacitor to OUT1A is required

Pin No.	Name	I/O	Function
36	/RESET	I	Active low to reset WA20-5822, Schmitt trigger input, Pull-down
37	DVDD	P	Regulator output for Core block, 1.2V
38	NC	-	No connection
39	BCK	I	I^2S bit clock
40	GND_IO	P	Ground for digital interface I/O
	Thermal Pad	P	This pad should be connected to Ground

P = Power or Ground, I = Input, O = Output, I/O = Input / Output

6. Block Diagram



7. Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the Wellang Sales Office/Distributors for availability and specifications.

Parameter	Symbol	Reference	Value	Unit
DVDD, VDD_PLL voltage	$DVDD_{AB}$	DGND	-0.3 ~ 1.5	V
VDD_IO voltage	VIO_{AB}	GND_IO	-0.3 ~ 5.25	V
Logic input voltage	VI_{AB}	GND	-0.3 ~ 5.25	V
Logic output voltage	VO_{AB}	GND	-0.3 ~ 5.25	V
PVDDXX voltage	$PVDD_{AB}$	PGNDXX	30	V
OUTXX voltage	$VOUT_{AB}$	PGNDXX	-0.3 ~ PVDDXX	V
BSTXX voltage	$VBST_{AB}$	OUTXX	-0.3 ~ 6.0	V
VDRX voltage	VDR_{AB}	AGND	-0.3 ~ 6.0	V
Junction Temperature	T_{JMAX}		160	°C
Storage Temperature	T_{STG}		-55 ~ +150	°C

8. Recommended Operating Condition

If Military/Aerospace specified devices are required, please contact the Wellang Sales Office/Distributors for availability and specifications.

Parameter	Symbol	Value	Unit
VDD_IO voltage	VDD_{IO}	3.0 ~ 3.6	V
PVDDXX voltage	PVDD	5 ~ 26.4	V
Operating Ambient Temperature	T_A	-25 ~ +85	°C
Load impedance (BTL) with (10uH+470nF) filter	$LOAD_{BTL}$	6 ~ 8	Ω
Load impedance (PBTL) with (10uH+470nF) filter	$LOAD_{PBTL}$	4	Ω

9. Electrical Characteristics

T_A = 25°C, VDD_{IO} = 3.3V, PVDDXX = 24V, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic Block						
Input High voltage	V_{IH}		2.31		3.6	V
Input Low voltage	V_{IL}		-0.3		0.8	V
Schmitt trig. Low to High threshold point	V_{T+}		2		3.6	V
Schmitt trig. High to Low threshold point	V_{T-}		-0.5		0.8	V
Input current	I_I	V_{IN}=V_{IL} MAX, DVDD=MIN	-50			uA
		V_{IN}=V_{IH} MIN, DVDD=MIN			50	uA
Input leakage current	I_L	V_{IN}=VSS, DVDD=MIN	-10		10	uA
Output Low voltage	V_{OL}	I_{OL} = -4mA	0		0.4	V
Output High voltage	V_{OH}	I_{OH} = 4mA	2.4		3.6	V
LDO output voltage	V_{LDO}	DVDD	1.08		1.32	V
Driver Block						
Current consumption	$I_{CC.VDDIO}$	VDD_IO=3.3V, No Input, No Load		35		mA
	$I_{CC.PVDD}$	PVDD=24V, No Input, 8Ω Load with 10uH inductor		40		mA
Peak current limit	I_{OCP}			6		A
Thermal shutdown temperature	T_{SD}			150		°C
Under voltage lockout	V_{UVP}			4.2		V
VDRX voltage	V_{VDR}		4.7	5.1	5.5	V
Speaker Amplifier						
SNR	SNR	A-Weighting filter		103		dB
THD+N	THD	P_{OUT}=1W, R=8Ω		0.09		%
Cross talk	Xtalk	1kHz		-96		dB

9. Electrical Characteristics (Continued)

T_A = 25°C, VDD_{IO} = 3.3V, PVDDXX = 24V, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
I²C Control Port						
SCL Clock Frequency	f_{SCL}		-		400	kHz
Hold Time Start Condition	t_{HDSTA}		600		-	ns
SCL Low Time	t_{LOW}		1300		-	ns
SCL High Time	t_{HIGH}		600		-	ns
Rise Time of SDA and SCL signals	t_{RISE}		-		300	ns
Fall Time of SDA and SCL signals	t_{FALL}		-		300	ns
Setup Time for STOP Condition	t_{SUSTO}		600		-	ns

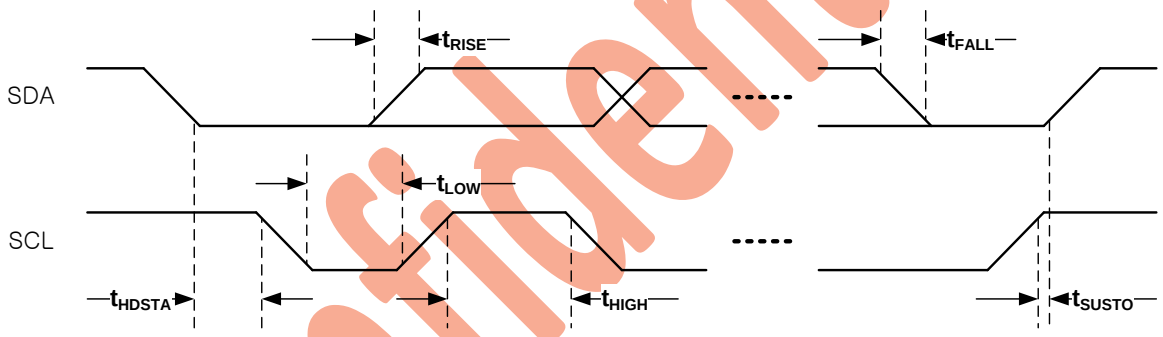


Figure 1. I²C Mode Timing Diagram

9. Electrical Characteristics (Continued)

T_A = 25°C, VDD_{IO} = 3.3V, PVDDXX = 24V, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
I²S Audio Interface						
BCK high time	t_{BH}		20		-	ns
BCK low time	t_{BL}		20		-	ns
SDATA setup time before BCK rising edge	t_{DS}		10		-	ns
SDATA hold time after BCK rising edge	t_{DH}		10		-	ns
WCK setup time before BCK rising edge	t_{WS}		20		-	ns
BCK rising edge before WCK edge	t_{WH}		20		-	ns

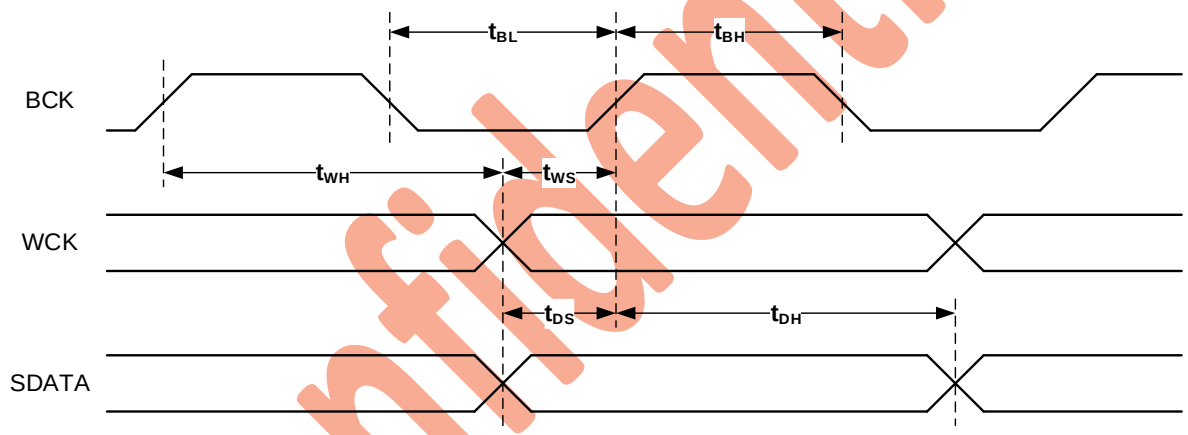


Figure 2. I²S Audio Interface Timing Diagram

10. Functional Description

I²C BUS OF WA20-5822

The WA20-5822 uses an industry standard Inter IC Control (I²C) bus to communicate with host IC. A host IC can write or read internal registers of the WA20-5822 via the I²C bus.

- General Description of I²C Bus

The I²C bus uses two signal lines – a serial clock line (SCL) and a serial data line (SDA) to communicate between integrated circuits in a system. Because the SDA line is open-drain type port, both the WA20-5822 and a host IC can only drive these pins low or leave them open.
In I²C bus, a master device means the device which generates serial clock on the SCL. A slave device means the device which receives serial clock. There can be many master and slave devices on an I²C bus. But, when one master device works on the bus, the other master devices should not generate signal on the lines. These unexpected interrupts can make other slave devices to fail to communicate with the mater device.
The WA20-5822 supports only slave mode of I²C bus. So, the WA20-5822 always receives serial clock from a host IC. The slave mode is enough to write/read data to/from the WA20-5822.

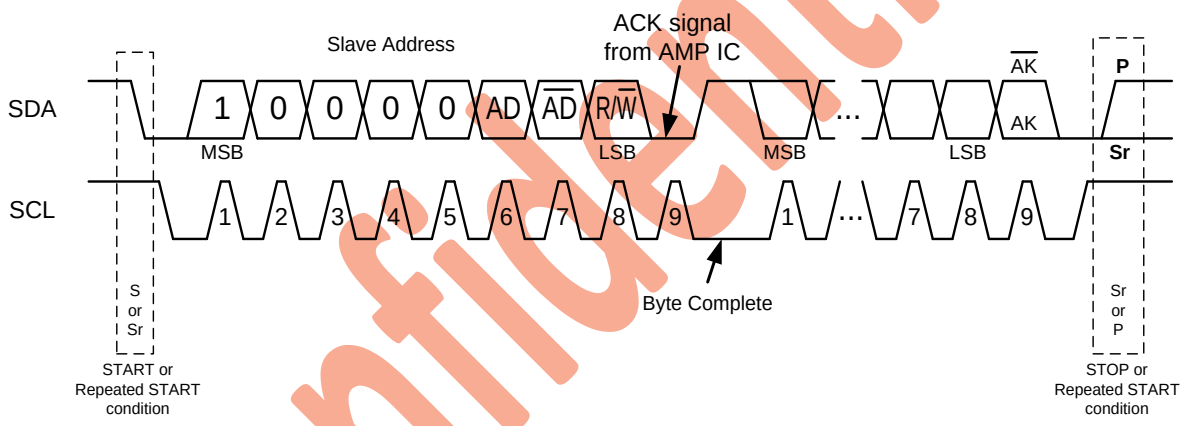


Figure 3. Basic Signaling Elements of I²C Bus

If there is no communication on I²C bus, two signal lines must keep in high state. I²C bus begins a communication with the start condition and ends a communication with the stop condition. The start condition can be generated by changing the SDA state high to low, during the SCL state remains in high. The stop condition can be generated by changing the SDA state low to high during the SCL remains in high state. Be aware that the stop condition always reset the internal status of I²C bus control logic. Except these two conditions, the SDA may not change during the SCL in high state. Otherwise, any abnormal start or stop condition will be generated.
I²C bus transfers the MSB on 1st data slot and the LSB on 8th data slot. I²C bus checks success or failure of every 1 byte transmission. The device which found an expected data on SDA must generate acknowledgement (keep low on SDA) on 9th clock. If there is no acknowledgement on 9th clock, the device which generated a data on SDA may stop transfer. Last 8th bit of the 1st byte is used to indicate whether the master device want to write or read data.
The WA20-5822 will generate an acknowledgement for every successful data transfer of 1 byte in write mode. On the contrary, in read mode the WA20-5822 will not generate an acknowledgement because data is generated by the WA20-5822. In this case, the WA20-5822 will check SDA state on 9th clock that the master device received a read data properly.

- Writing Operation

When last 8th bit of the 1st byte is set to low state, the writing operation of I^2C bus begins. The WA20-5822 supports 2 kind of writing operations which presented on Figure 4.
The type presented on Figure 4-(a) is single byte write operation. "Sub Address" on 2nd byte means the internal register address of the WA20-5822. The "Data" on 3rd byte will be written into the internal register address on "Sub Address". If stop condition is not generated, writing "Data" on specific "Sub Address" can be repeated like Figure 4-(b). "Data #n" will be written on "Sub Address #n".

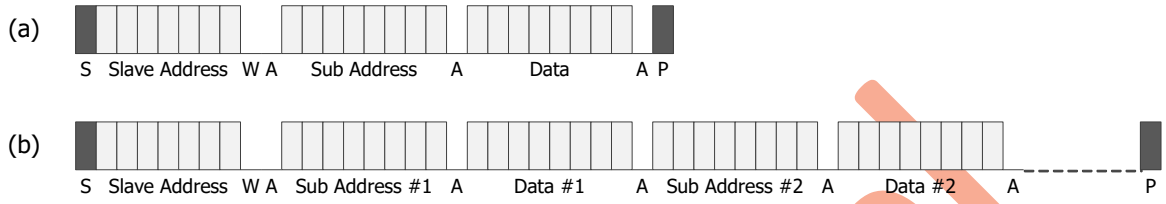


Figure 4. Single Byte Write Mode Sequence

Figure 5-(a) and Figure 5-(b) represent 4 byte writing operations in order to configure 32-bit floating point coefficients which are used as PEQ filter coefficients, DRC QMF filter coefficients, and various gains.
The difference between 4 byte writing operation and single byte writing operation is only the size of transferring data. So, after sending "Sub Address", 4 sequential bytes must be transferred from the MSB (most significant byte) to the LSB (least significant byte) sequence.

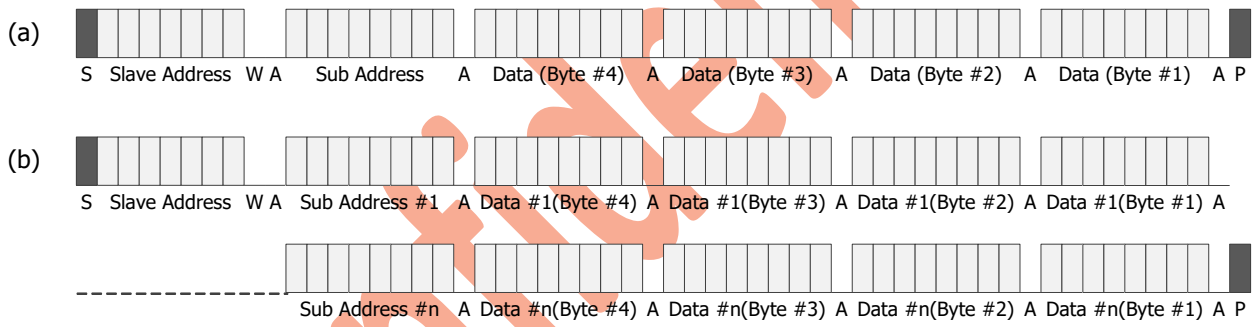


Figure 5. Quad Byte Write Mode Sequence

Each Bi-Quad filter uses 5 coefficients as shown in Figure 13. Any unexpected coefficient value changes on any part of 5 coefficients can generate unstable Bi-Quad filter response. For example, if only one of 5 coefficients for a Bi-quad filter is changed and downloaded, its combined 5-coefficient set can have unstable operation while old and new coefficients are mixed together. Therefore, to prevent this kind of problem, the WA20-5822 writes coefficients to coefficient registers only when the last 5th coefficient of each Bi-quad filter is downloaded, which means all of 5 coefficients are fully ready.

- Reading Operation

Figure 6 represents single byte reading operation from the WA20-5822. To read data from the WA20-5822, generate the start condition to begin a transmission and send both "Slave Address" with write mode flag and "Sub Address". After then by regenerating the start condition (Sr) again and transferring "Slave Address" with read mode flag, reading operation begins. The WA20-5822 will generate data on SDA signal synchronizing with serial clocks on the SCL. Because the SDA signal generated from the WA20-5822, the master device must generate ACK on 9th slot to confirm that the master received 1 byte successfully.
In case of one byte reading operation, NAK (not acknowledged) signal must be generated. Finally, the stop condition follows to end a transmission.

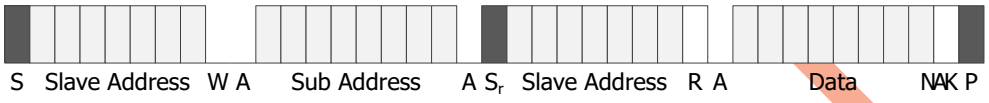


Figure 6. Single Byte Read Mode Sequence

Figure 7 represents quad byte reading operation. The difference between quad byte reading operation and single byte reading operation is only the size of receiving data. So, after sending "Sub Address", 4 sequential bytes must be received from the MSB to the LSB sequence.

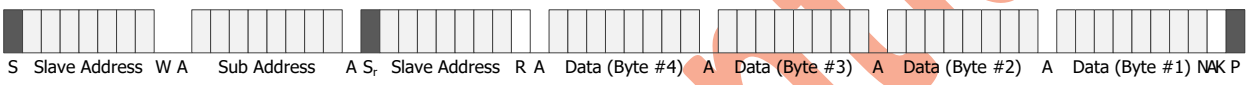


Figure 7. Quad Byte Read Mode Sequence

- I²C Glitch Filter

To clean out the threats of noise in today's high-speed-board system, the WA20-5822 has a glitch elimination filter on the I²C ports. Glitches in the transmission lines of the I²C port can be safely removed with this function. Please refer to the address 0xAE register.

- I²C Slave Address

The WA20-5822 supports up to four slave addresses. A master device sends the target slave address on the 1st byte after the start condition in order to communication with other integrated circuits. MSB 7 bits of the 1st byte data are used for the slave address. So, four WA20-5822s can be connected to the same I²C bus at the same time. For multi-chip operation, use the proper I²C slave address According to AD pin and the initial state of MONITOR_1 pin as shown in Table 1.

Table 1. I²C Slave Address

Pin Name			
AD	MONITOR_1		
Value	Pull-down (L)	Pull-up (H)	No PU / PD (default: L)
0	Addr : 0x82	Addr : 0x86	Addr : 0x82
1	Addr : 0x84	Addr : 0x88	Addr : 0x84

CLOCK, RESET & CONTROL

- System Clock

The on-chip PLL of WA20-5822 generates the internal system clocks using an external master clock. The WA20-5822 supports external master clock frequency from 3.072 MHz to 24.576MHz. For proper operation, the registers for PLL configuration should be set correctly According to master clock frequency (Address 0x06).

- Timing Sequence

For proper power up, initialization and power down of WA20-5822, it is recommend to use the following sequence as shown in Figure 8.

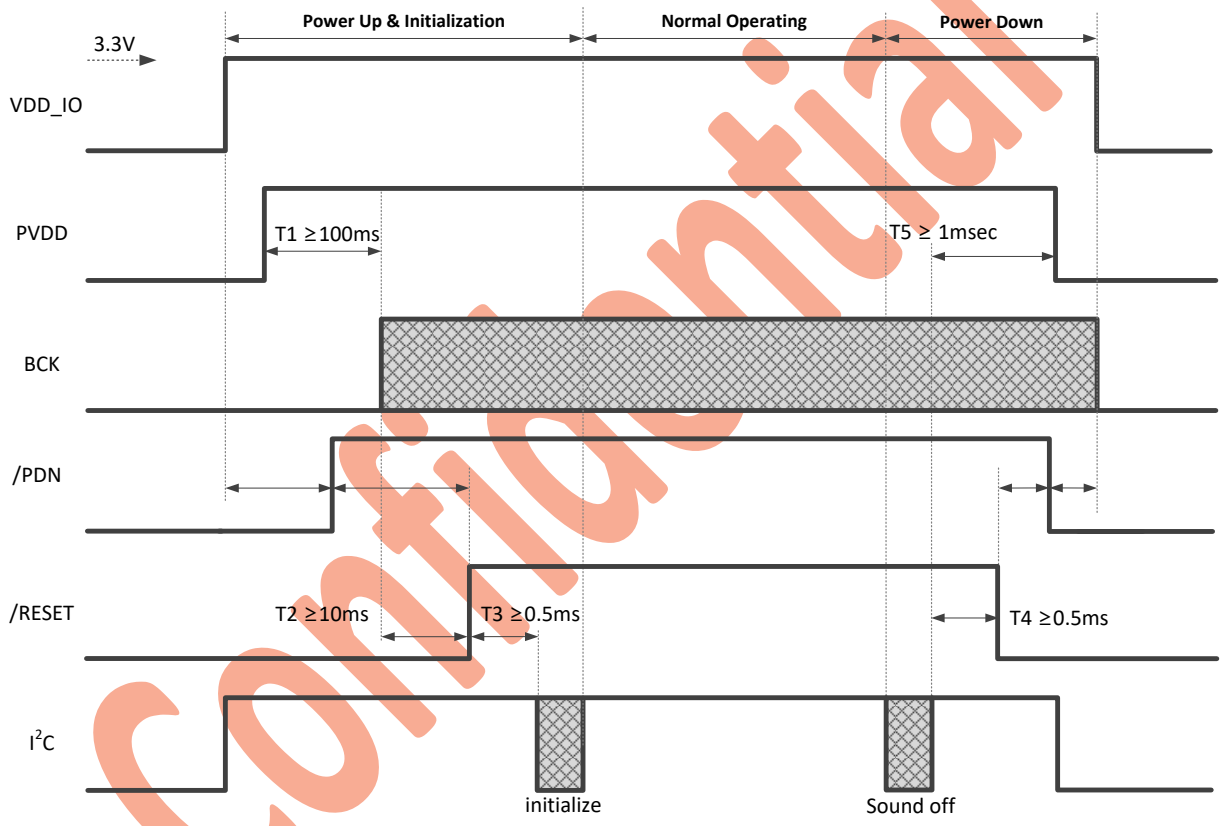


Figure 8. Recommended Timing Sequence

- Power-Up & Initialization Sequence

1) Ramp up VDD_IO to at least 3.3V.
2) Ramp up PVDD.
3) Drive /PDN = High between VDD_IO rising and /RESET rising.
4) Drive BCLK signal at least 100ms later after PVDD (T1 ≥ 100ms).
5) Drive /RESET = High at least 10ms later after BCK (T2 ≥ 10ms).
6) Wait for at least 0.5ms for I²C communication (T3 ≥ 0.5ms).
7) Execute both amp initialization sequence (e.g. clock, volume, DRC, PEQ setup) and sound on sequence.

- Power-Down Sequence

1) When both DC and AC power are on, make sure to execute sound off sequence.
2) Drive /RESET = Low at least 0.5 ms after sound off sequence (T4 ≥ 0.5ms).
3) Ramp down PVDD at least 1 ms later after sound off sequence (T5 ≥ 1ms).
4) Drive /PDN = Low between /RESET falling and VDD_IO falling.
5) Ramp down VDD_IO.

- Sound On/Off Sequence

For proper sound on/off of WA20-5822, use the following sequence as shown in Figure 9.

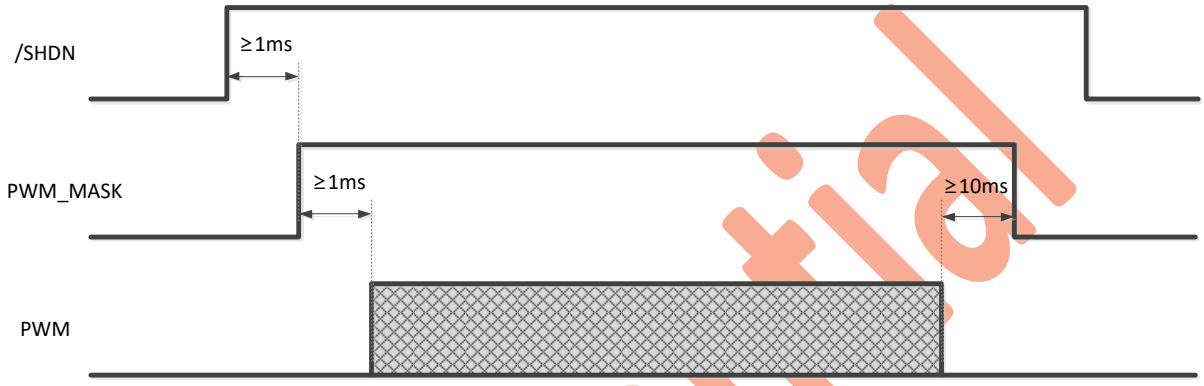


Figure 9. Sound On & Off Sequence

AUDIO INPUT

The WA20-5822 receives audio data through inter-IC sound (I^2S) or time division multiplexed (TDM) audio interface.

- I^2S Interface

I^2S interface uses 2 clock lines and 1 data line to receive the audio data. One of these clock lines is the WCK. A period of WCK is same with sampling period of audio data i.e. 64bits (32bits for each channel). One of the main functions of WCK defines the channels, the low state of WCK indicates the 1st channel i.e. left channel and the high state indicates the 2nd channel i.e. right channel. This feature enables the clock receiving device to synchronize the data word-wise for transmitting or receiving from clock generating device. The other clock line is BCK. This clock line is used to synchronize the bit-wise data. The number of BCK clock for one WCK period is 64.
The name of data transfer line is SDATA. The data being synchronized with BCK must be loaded on this line. The WA20-5822 receives data on rising edge of BCK. The bit range for I^2S is predefined.
The WA20-5822 can only work as a slave on bus. In slave mode, the WA20-5822 receives WCK and BCK from external source. Please refer the following Figure 10.

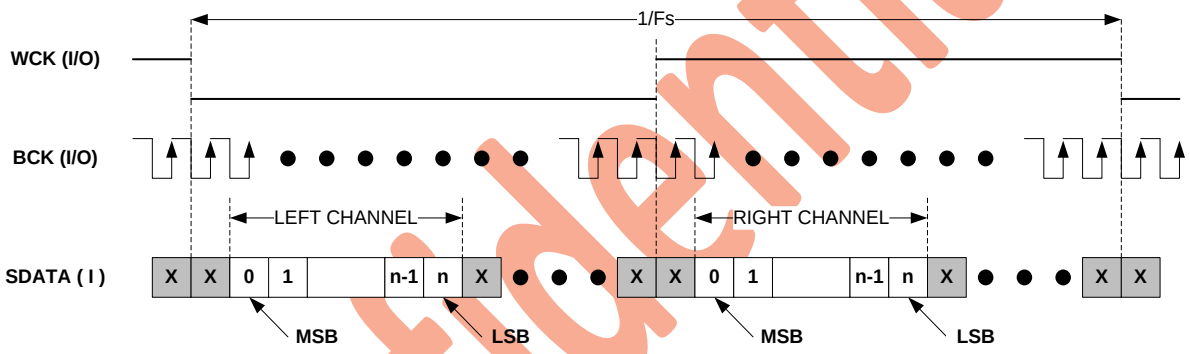


Figure 10. I^2S Audio Interface Format

- TDM Interface

While I²S interface transmits 2-channels of audio data, TDM (Time Division Multiplexed) interface allows multiple channels of audio data to be transmitted on a single data line. The TDM interface is similar to the 2-channel serial audio interface with the exception that more channels, typically 4, 6 or 8, are transmitted within a sample frame or sample period, as shown in Figure 11.
As with the 2-channel serial audio interface, the TDM interface is comprised of two control clocks, a frame synchronization pulse (FSYNC) and serial clock (SCLK), and the serial audio data line (SDATA).

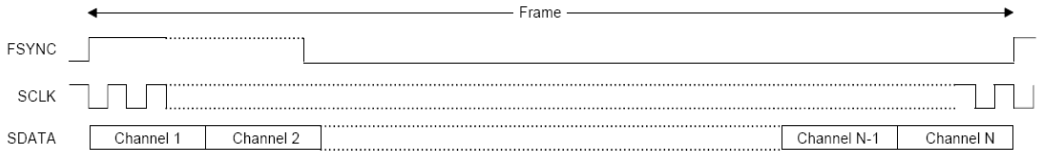


Figure 11. TDM Audio Interface Format

In order to reduce the number of chip pins, the WA20-5822 shares 2 clock lines and 1 data line between I²S interface and TDM interface as shown in Figure 12.

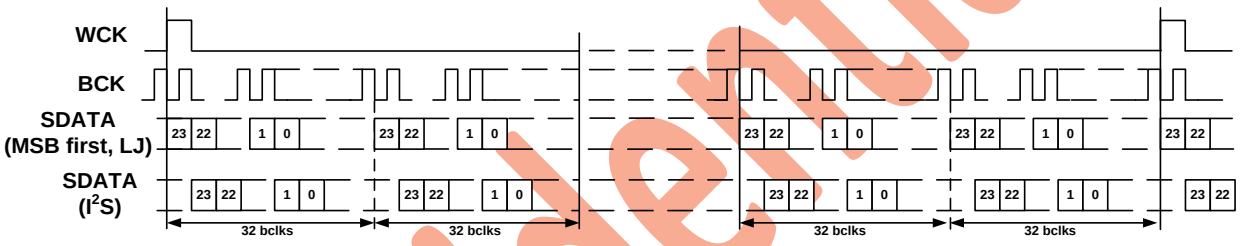


Figure 12. TDM Interface using I²S Interface Signal

- SDATA Generator

The SDATA generator of the WA20-5822 sends I²S out signal. In order for SDATA out process to function stably, the falling of BCK should either synchronize or occur ahead of falling or rising of WCK.
Refer to the configuration registers of SDATA generation (Address 0xB1 & 0xAD) in the Appendix A and refer to Chapter 9. Electrical Characteristics – Audio Interface.

Table 2. SDATA Generator Control

SDATA Generator Control	Register Value	
	0x0F	0xF0
Address 0xB1	SDATA Out → MONITOR_1 pin	SDATA out → MONITOR_2 pin

MIXER

Channel mixer can be used in lots of application needs like pseudo stereo and etc. User can mix input channels into each output channels with designated gains and polarity. Step size of mixer gain is variable according to the gain level as shown below.

Table 3. Variable Step Mixing Gain

Volume Range (dB)	Step (dB)
+18 ~ +6	1
+5.5 ~ -5.5	0.5
-6 ~ -32	1
< -32	-∞

In total, 4 mixing gain coefficients denoted as M00, M01, M10 and M11 are defined as shown in the equation below. Each Mxx stores volume value in dB scale, and the relation between register value and actual gain in dB is shown in the Appendix B. By default, each input channel is connected to each output channel directly; M00 and M11 are set as 0 dB in plus polarity, M01 and M10 are set as -∞ dB.

[Output Channels] = [Mixer Matrix] • [Input Channels]

$$\begin{bmatrix} CH1\ OUT \\ CH2\ OUT \end{bmatrix} = \begin{bmatrix} M00 & M01 \\ M10 & M11 \end{bmatrix} \bullet \begin{bmatrix} CH1\ IN \\ CH2\ IN \end{bmatrix}$$

Equation 1. Serial Mixer Matrix

In order to load mixer coefficients into internal memory, send the index value of the mixer gain table to the register address 0x09 ~ 0x0C. Each address matches to M00, M01, M10 and M11 sequentially.

Audio Enhancement Technology: MM Audio

The WA20-5822 has four audio enhancement features that improve listening experience: dialog clarity, loudness compensation, dynamic bass booster, and virtual expander. The functions of the audio enhancement can be controlled via the control registers of the address 0x0E ~ 0x16.

- Dialog Clarity

- Enhances overall vocal clarity in music and movies
- To improve vocal intelligence in the contents, Vocal and Environmental Sound Separation Algorithm is applied
- Best fit for news and drama contents
- It also gives great benefit for the tele-conferencing
- User can control the balance of Voice and Environmental Sound to find the best performance

- Loudness Compensation

- The human listening perception varies across frequencies as well as absolute sound pressure level (SPL)
- It needs to compensate lower and higher frequencies versus mid-range to give an equal tonal balance to the listeners at different volume levels
- The amount of loudness compensation is different at each volume level in Accordance with the equal-loudness contour
- User can set the threshold SPL and maximum compensation level as well as cut-off frequencies of low and high bands

- Dynamic Bass Booster

- Conventional EQ based bass booster may cause severe distortion
- Psycho-acoustic approach also makes audible harmonics (intentional noises), and it affects sound quality negatively
- Dynamic Bass Booster automatically controls output gain across user's volume setup, retaining the maximum excursion of speaker driver within the dynamic range
- By dynamically controlled gain in low frequencies, low level signals can be amplified without distortion while peak signals are unaffected, preventing overload of the amplifier and speakers
- User can set the crossover frequency to extend lower range and its maximum boosting level
- User also can adjust the cut-off frequency and slope of high-pass filter by -6 ~ -36dB/octave to remove mechanical vibrations or chassis rattling

- Virtual Expander

- Immersive sound effect with stereo speakers using the low complexity transaural technology of pseudo-HRTF
- Panoramic surround effect smoothly extends the sound field we well as spatial depth
- Versatile user setup menu covers various geometrical conditions between speakers and listener
- User can design well balanced spatial sound manipulating center and surround gain combination
- It gives dramatic virtual effect to the front-firing speaker products, such as TV, PC Monitor, Soundbar, and any type of stereo sound devices

PRE-PROCESSING

- Bi-Quad Filter Chain

The Bi-Quad filter means 2nd order IIR filter. The WA20-5822 contains a serial chain of Bi-Quad filters with proprietary floating point operation schemes. The Bi-Quad filter chains can be used in various purposes; loudness control, parametric EQ, loud-speaker EQ, and etc. The Bi-Quad filter structure (direct 1 form) is shown in Figure 13.

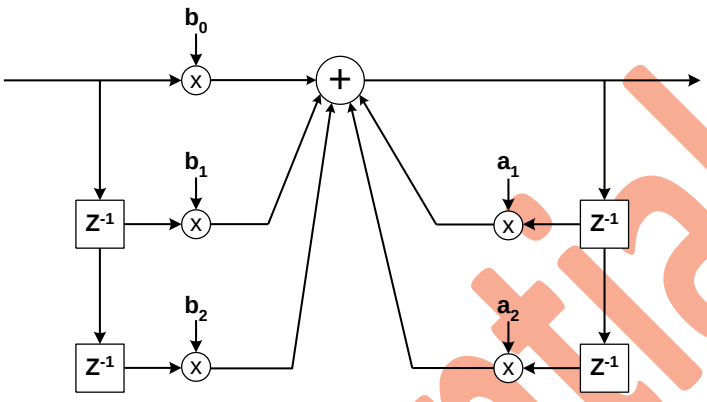


Figure 13. Bi-Quad Filter Structure

Twenty Bi-Quad filters are linked serially for one channel. As shown in Figure 14, first three filters (BQ1 ~ BQ3) can be used for loudness control. From BQ1 to BQ11, each filter can be configured differently over channel 1 and 2. And the others (BQ12 ~ BQ20) are configured equally over channel 1 and 2. Additionally, the position of BQ9 ~ BQ14 can be moved behind DRC operation According to the configuration register (Address 0x2E).

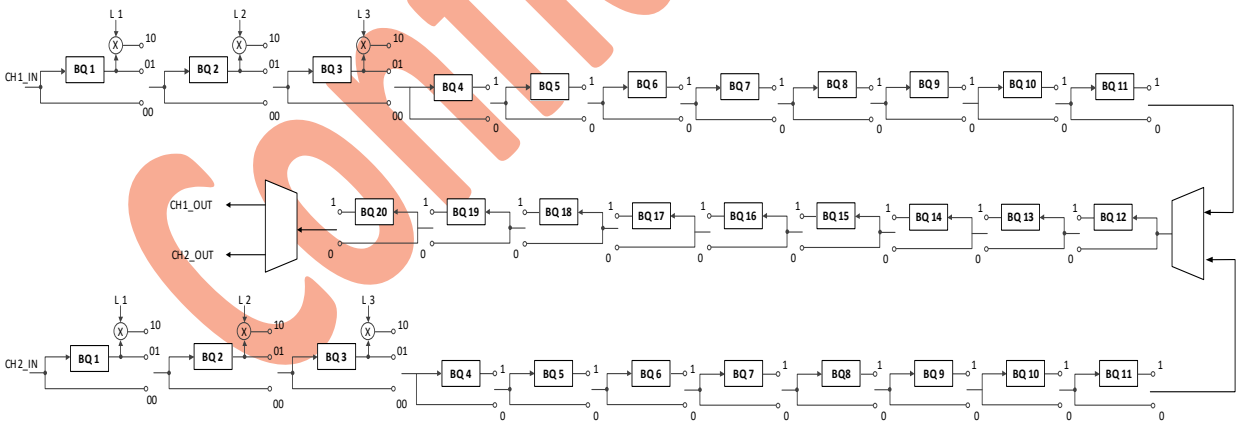


Figure 14. Bi-Quad Filter Chain

Filter coefficients are 32-bit floating point numbers and can be downloaded through I2C interface. To download Bi-Quad filter coefficients to the WA20-5822, select download channel by using CH flag in register address 0x7E first. Then, write actual coefficient values to register addresses, from 0x00 to 0x63 in the coefficient register addresses.

The coefficient mode register addresses from 0x00 through 0x04 designate the five coefficients of the first Bi-Quad (BQ1) filter and represent coefficients b0, b1, b2, a1, a2 respectively. The coefficient mode register addresses from 0x05 through 0x09 designate coefficients of the 2nd Bi-Quad (BQ2) filter, and so on. The enable/disable operation of these Bi-Quad filters can be made by using BQF flag in register addresses of 0x20 ~ 0x29. Table 4 shows the coefficient mode register address of each Bi-Quad filter.

Table 4. Address of Coefficients for Bi-Quad Filter Chain

Coefficient Mode Register Addr.	**0x00 ~ 0x04**	**0x05 ~ 0x09**	**0x0A ~ 0x0E**	**0x0F ~ 0x13**	**0x14 ~ 0x18**	**0x19 ~ 0x1D**
Addr. 0x7E = 0x81 Addr. 0x7E = 0x82	CH1 BQ1 CH2 BQ1	CH1 BQ2 CH2 BQ2	CH1 BQ3 CH2 BQ3	CH1 BQ4 CH2 BQ4	CH1 BQ5 CH2 BQ5	CH1 BQ6 CH2 BQ6

Coefficient Mode Register Addr.	**0x1E ~ 0x22**	**0x23 ~ 0x27**	**0x28 ~ 0x2C**	**0x2D ~ 0x31**	**0x32 ~ 0x36**	
Addr. 0x7E = 0x81 Addr. 0x7E = 0x82	CH1 BQ7 CH2 BQ7	CH1 BQ8 CH2 BQ8	CH1 BQ9 CH2 BQ9	CH1 BQ10 CH2 BQ10	CH1 BQ11 CH2 BQ11	

Coefficient Mode Register Addr.	**0x37 ~ 0x3B**	**0x3C ~ 0x40**	**0x41 ~ 0x45**	**0x46 ~ 0x4A**	**0x4B ~ 0x4F**	**0x50 ~ 0x54**
Addr. 0x7E = 0x81	BQ12	BQ13	BQ14	BQ15	BQ16	BQ17

Coefficient Mode Register Addr.	**0x55 ~ 0x59**	**0x5A ~ 0x5E**	**0x5F ~ 0x63**			
Addr. 0x7E = 0x81	BQ18	BQ19	BQ20			

- Loudness Control

The WA20-5822 provides loudness control function using coefficient values. Loudness control means the compensation of frequency characteristics in low volume level to fit the acoustic characteristics of human ears.

As shown in Figure 14, loudness control can be performed using 3 Bi-Quad filters with loudness gains which are applied equally over two channels. Table 5 shows the coefficient mode register address of each gain.

Table 5. Address for Loudness Gain

Coefficient Mode Register Addr.	**0x3F**	**0x40**	**0x41**
Addr. 0x7E = 0x87	Loudness Gain 1	Loudness Gain 2	Loudness Gain 3

VOLUME & DYNAMIC RANGE CONTROL

Master and channel volumes of the WA20-5822 are independently controlled and softly changed. The register address 0x1C is the master volume control that affects both channels simultaneously and the register address 0x1E and 0x1F correspond to the channel volume control for channel 1 and 2 respectively. The possible maximum gain is +48.375dB with using master volume fine control, master volume and channel volume because the master volume applies the gain to an input signal independent from a channel volume. However, in such a case, a clipping might occur to prevent a signal overflow error if the magnitude of the input signal is large enough to exceed 0dB under the combined volume setting.

- Master Volume Control

By setting volume control register (Address 0x1C), master volume is controlled from negative infinity through 0dB with selectable step size as follows. For details on the master volume setting, see the register value Table 12 shown in Appendix B.

Table 6. Level Dependent Master Volume Steps

Step	Range
0.5dB	0 ~ -125dB

- Channel Volume Control

By setting volume control registers (Address 0x1E and 0x1F), channel volumes are independently controlled from negative infinity through +48dB with two selectable step sizes as described below, and in the Appendix B, exact values for channel volume setting are described.

Table 7. Level Dependent Channel Volume Steps

Step	Range
0.5dB	+48 ~ -79dB

- Master Volume Fine Control

Fine control for master volume is possible (+0.125dB step up to maximum +0.375dB boost). Refer the register address 0x1D in the Appendix A.

- Mute and Soft Volume Change

The WA20-5822 enters mute state by setting soft mute flag of register address 0x6A. Soft mute is implemented so that the volume gradually increases or decreases when mute is turned off or on respectively. Also, the soft mute speed and soft volume change speed rates are programmable. Designers can minimize the pop noise by controlling the soft mute speed and volume change intervals. Refer SM flag of register address 0x6A and SVI flag of register address 0x1A.

- Auto Mute

The WA20-5822 can mute the sound automatically when the level of input audio signal is lower than the register-controlled threshold value. The mute can be done by PWM switching with 50 % duty ratio in AD mode or BOW width high in BD mode as shown in Figure 17. Auto mute is supported for internal channels 1~2 after 2x2 mixer block. Refer register address 0x6B.

- Accelerated Dynamic Range Control (AccDRC)

The WA20-5822 has a dynamic range control, which comprises a high band DRC, a low band DRC, and a sub band DRC. The input data is filtered by HPF, LPF and SPF, and then processed by H-DRC, L-DRC, and S-DRC respectively. Three processed results are merged into a single data. For detailed setting of the DRC registers, please refer to the register addresses in Table 8.

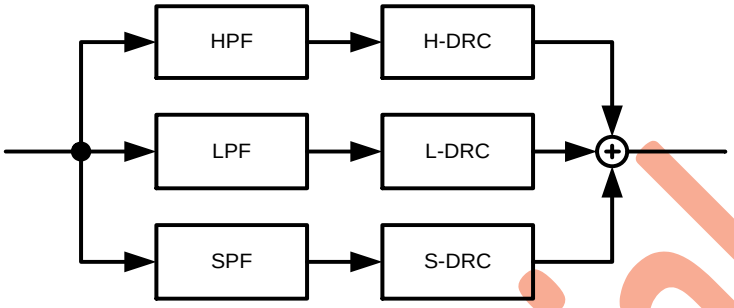


Figure 15. Block Diagram of Dynamic Range Control

Table 8. Coefficient Register Map for Dynamic Range Control

Coefficient Mode Register Addr.	0x00 ~ 0x04	0x05 ~ 0x09	0x0A ~ 0x0E	0x0F ~ 0x13	0x14 ~ 0x18	0x19 ~ 0x1D
Addr. 0x7E = 0x86	LPF 1 of L-DRC	LPF 2 of L-DRC	HPF 1 of H-DRC	HPF 2 of H-DRC	SPF 1 of S-DRC	SPF 2 of S-DRC

The WA20-5822 has a new DRC scheme called as AccDRC function, and it manipulates an excessive level of input signals while configuring more flexible parameters of attenuation and recover operations. In the attenuation process, 2-step attenuation rate can be applied depending on the relation between the threshold level and the input signal level. When the input signal level is too high, the first attenuation process usually decreases the input in a short period so as to avoid distortion, and the second attenuation reduces the signal level with a little longer time. The recovering operation can be skipped depending on its configuration while the attenuation process is done repeatedly in a short period.

Please refer to the register address 0x5C ~ 0x5E and the following table for additional parameters. In addition, the AccDRC uses coefficient registers as shown in Table 9.

Table 9. Coefficient Register Map for AccDRC

Coefficient Mode Register Addr.	0x0A ~ 0x0C	0x0F ~ 0x11	0x14 ~ 0x16	0x19 ~ 0x1B
Addr. 0x7E = 0x87	Peak Envelope Para. of each DRC band	Threshold Para. of each DRC band	Attack Para. of each DRC band	Release Para. of each DRC band

Coefficient Mode Register Addr.	0x1E ~ 0x20	0x23 ~ 0x25	0x28 ~ 0x2A	0x2D ~ 0x2F
Addr. 0x7E = 0x87	AccThreshold Para. of each DRC band	AccWeight Para. of each DRC band	RSWindow Para. of each DRC band	Inv_AccThd Para. of each DRC band

Coefficient Mode Register Addr.	0x32 ~ 0x34	0x37 ~ 0x39
Addr. 0x7E = 0x87	Release Delay Threshold Para. of each DRC band	Attack Flag Para. of each DRC band

- Limiter

The limiter prevents the merged DRC output of each frequency band from exceeding a preset threshold value. Please refer to the register address 0x5F and the following table for relevant parameters.

Table 10. Coefficient Register Map for Limiter

Coefficient Mode Register Addr.	0x0D	0x12	0x17	0x1C
Addr. 0x7E = 0x87	Peak Envelope Para. of Limiter	Threshold Para. of Limiter	Attenuation Para. of Limiter	Recover Para. of Limiter

Coefficient Mode Register Addr.	0x21	0x26	0x2B	0x30
Addr. 0x7E = 0x87	AccThreshold Para. of Limiter	AccWeight Para. of Limiter	RSWindow Para. of Limiter	Inv_AccThd Para. of Limiter

Coefficient Mode Register Addr.	0x35
Addr. 0x7E = 0x87	Recover Delay Threshold Para. of Limiter

- Power Meter

The power meter measures the energy of the internally processed signal, and its value is Accessed via the register of address 0xA7. The measured value can be read through the register of address 0xA8. (Refer to the Table 16 of Power Meter)

As audio signals change very rapidly considering the time required for Accessing the I^2C, a user can set the power meter gain to obtain relatively stable values. The power meter gain controls the decaying speed of the instantaneous peak value. For instance, if the power meter gain is set close to one, the measured value of the power meter will decay much slower. On the contrary, if the power meter gain is relatively small, the measured value will decay very fast, and it will be renewed more frequently.

The power meter gain is a 32-bit floating point number and can be downloaded through I^2C interface. Table 11 shows the coefficient mode register address of the power meter gain.

Table 11. Address for Power Meter Gain

Coefficient Mode Register Addr.	0x3B
Addr. 0x7E = 0x87	Power Meter Gain

OUTPUT INTERFACE

- Output Configuration

The output of WA20-5822 has various options. To produce proper output signal, register address 0x7B, 0x75, 0x8E, 0x8F and 0x85 should be set to appropriate values.

- PWM Output Mapper

Any internal channel that produces a PWM output can be assigned to any PWM output hardware port (or pin) by mapping output port register. This feature is very helpful for the hardware designer because it can relieve difficulties in the power stage signal routing and channel assignment if the output channel order is fixed. See the register address 0x8E and 0x8F in the Appendix A.

- Switching Output Mode

There are two selectable switching output modes in the WA20-5822. The difference between two output modes lies in the relationship of the relative signal pattern between PWM OUTxA and PWM OUTxB for a channel x.

The first one is called as AD mode. In AD mode, A output and B output of each PWM output pair are mutually complementary. So, this can be applied to both half bridge and full bridge output stage.

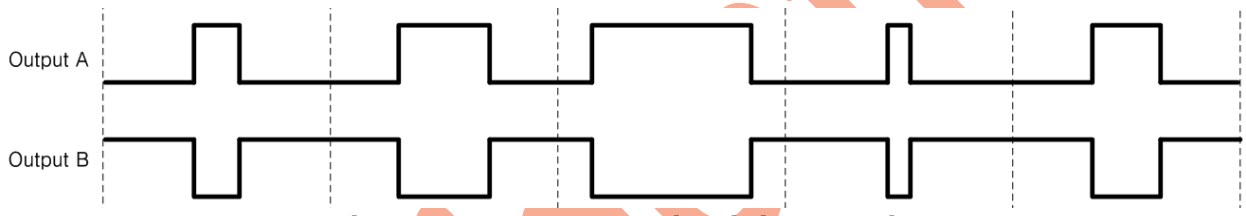


Figure 16. PWM Output Signals in AD Mode

The other one is called as BD mode. This mode is applied to only BTL speaker configuration. An example of output signals in BD mode is shown in Figure 17.

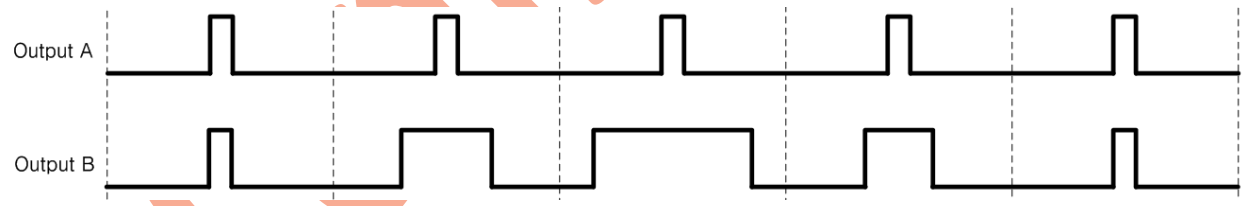


Figure 17. PWM Output Signals in BD Mode

- Soft Start

The soft start reduces pop noise by controlling rapidly increased energy of PWM in AD mode. To begin soft start operation, PWM soft start enable register (Address 0x90: PSE) should be set to high, and then PWM switching on/off register (Address 0x7B: PON) should be set to low. The duty ratio of PWM output increases from 127:1 (Low:High) to 50:50 (Low:High). Step repeat time register (Address 0x90: SRT) means repeat number of PWM output in one duty sector. Soft start operation with 17 repetitions is shown in the Figure 18.

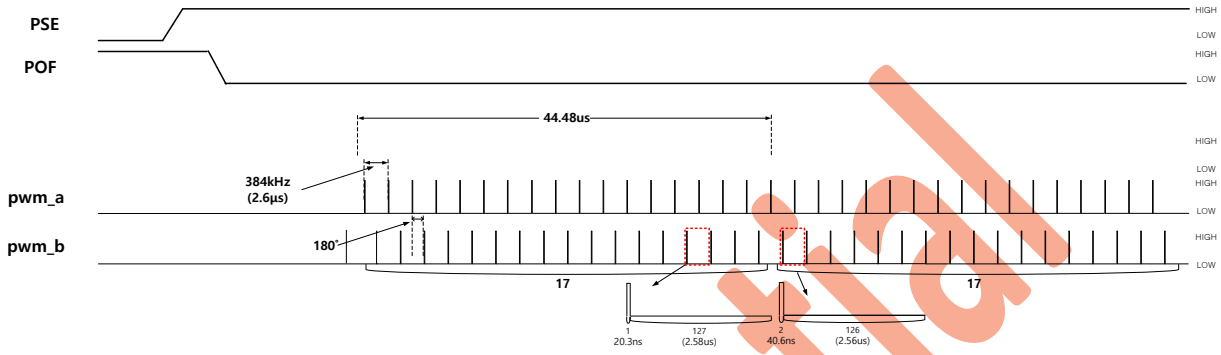


Figure 18. Soft Start Operation Timing

DC PROTECTION

This DC protection block prevents the system from outputting DC signal, which can cause a speaker unit burnt. Three sub functions are employed to prevent DC output, which are monitoring a memory checksum, observing a modulation index, and cutting DC output via hard-wired filters. Except for the hard-wired DC cut filter, the other two blocks only report the error status, and external MCU may reset the amplifier chip by setting the DC soft reset register to high.

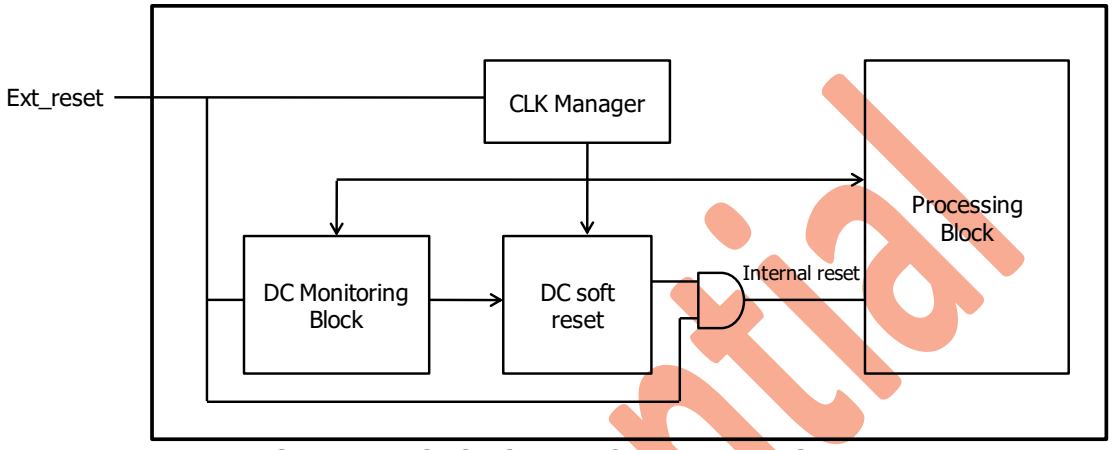


Figure 19. Block Diagram for DC Protection

- Memory Checksum

The checksum data of coefficients are 32-bit floating point numbers and can be downloaded through I^2C interface. This memory checksum block compares the checksum data of current memory block and the checksum data at the initial time. If it happens a discrepancy between two values due to some memory fault, the error flag of address 0x9F is set to high. The external MCU can monitor this error flag and reset the chip by setting the soft reset to high at address 0x04. This soft reset will initialize the whole chip, and initialization process of the memory should be done thereafter.

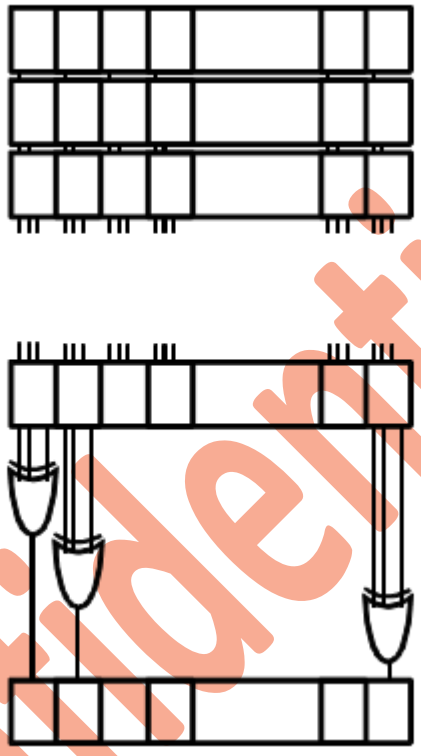


Figure 20. Structure of Memory Checksum

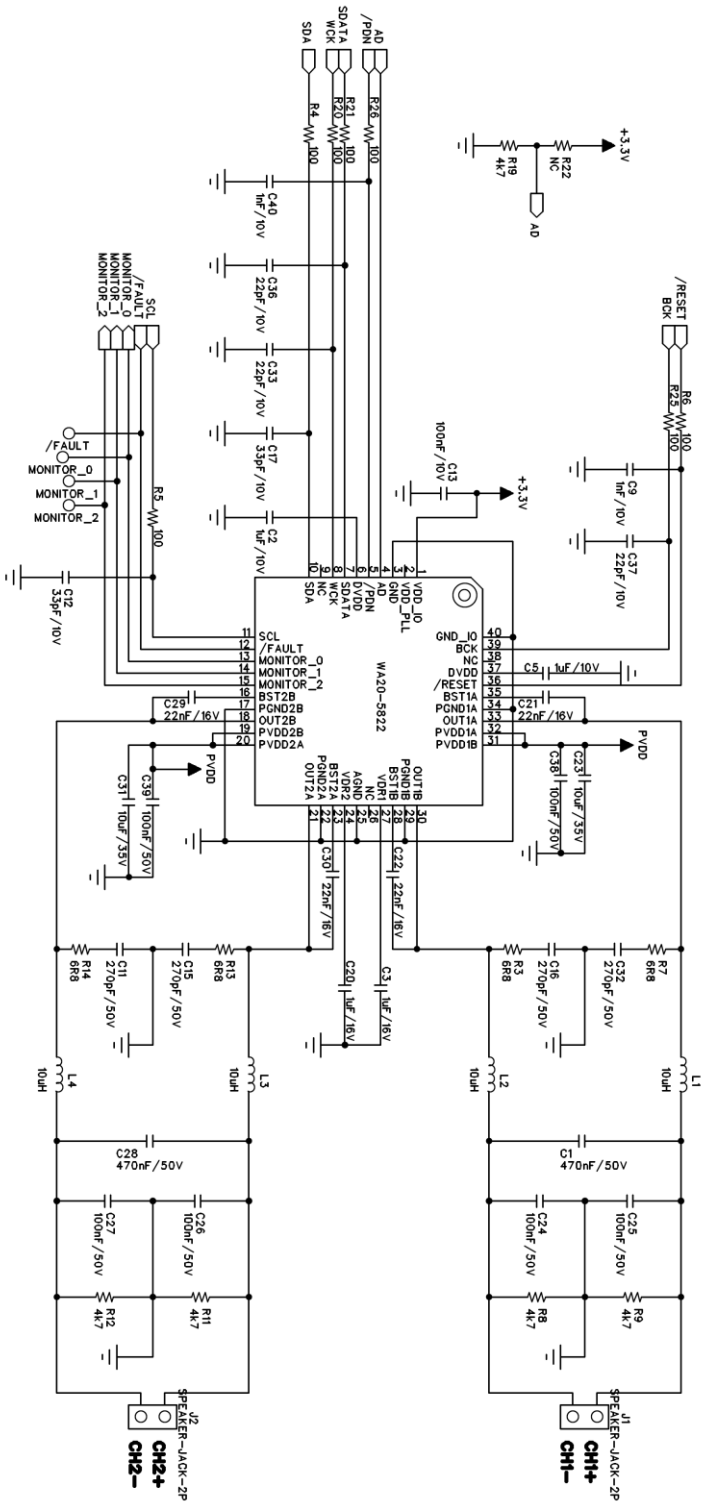
- Modulation Index Check

When there is a DC component in the output, the modulation index tends to stay over or under certain value. The modulation index check block constantly monitors the PWM modulation index, and if the index value continues to stay over or under certain period of time, it sets modulation index error flag of address 0x9F to high. The PWM modulation duty at address 0x93 and 0x94 can be set to decide the level of DC monitoring for AD and BD mode respectively.

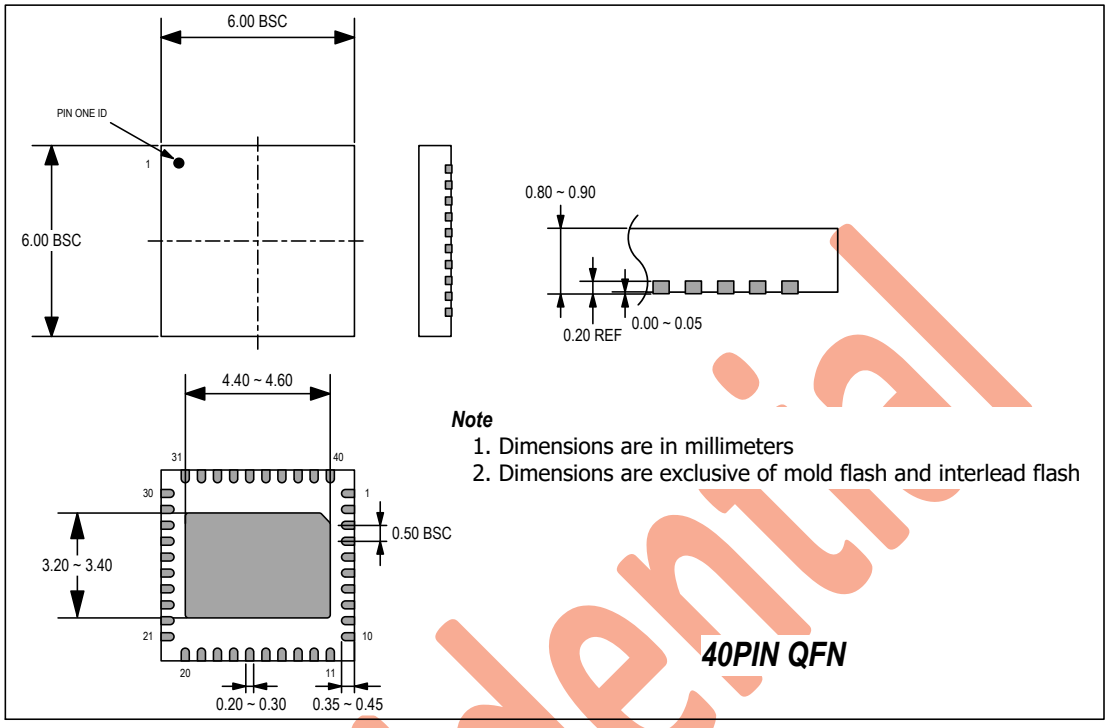
- Hard-wired DC cut

The hard-wired DC cut filters prevent the system from outputting the signal of less than 1Hz frequency. This filter is implemented using a Bi-quad filter.

11. Application Circuits



12. Package Outline



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14. Contact information

For sales information	snm@wellang.com
For additional information	http://www.wellang.com

15. Appendix

A. Configuration Register Summary

Addr 0x00: Audio Input Format

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	IF

Name	Description	Value	Meaning	Ref.
IF	Input Format	**b'0**	I^2S, Slave mode	
		b'1	General Serial Audio, Slave mode	

Addr 0x01: General Serial Audio Format

Bit	7	6	5	4	3	2	1	0
Name	X	X	BCKS		BS		SBO	LRJ

Name	Description	Value	Meaning	Ref.
LRJ	Serial Data Justify	**b'0**	Left justify	
		b'1	Right justify	
SBO	Serial Bit Order	**b'0**	MSB first	
		b'1	LSB first	
BS	Serial Bit Size	**b'00**	24 bit	
		b'01	20 bit	
		b'10	32 bit	
		b'11	16 bit	
BCKS	Bit Clock Size Select	**b'00**	64 BCK/WCK	
		b'01	48 BCK/WCK	
		b'10	32 BCK/WCK	
		b'11	128 BCK/WCK	

Addr 0x02: TDM Audio Format0

Bit	7	6	5	4	3	2	1	0
Name	TDM	FSYNC_INV	FSYNC_SHIFT	X	TDM_SEL		TDM_DEV_NO	

Name	Description	Value	Meaning	Ref.
TDM_DEV_NO	Number of TDM devices	**b'00**	2 devices(4CH)	
		b'01	3 devices(6CH)	
		b'10	4 devices(8CH)	
TDM_SEL	TDM device selection.	**b'00**	1st Device	
		b'01	2nd Device	
		b'10	3rd Device	
		b'11	4th Device	
FSYNC_SHIFT		**b'0**	No offset of audio data in the audio frame	
		b'1	1 BCK offset of audio data in the audio frame	
FSYNC_INV		**b'0**	Audio data starts at the rising edge of FSYNC	
		b'1	Audio data starts at the falling edge of FSYNC	
TDM	TDM mode	**b'0**	Normal mode	
		b'1	TDM mode	

Addr 0x03: TDM Audio Format1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	TDM_BS	

Name	Description	Value	Meaning	Ref.
TDM_BS	Serial Bit Size	b'00	24 bit	
		b'10	32 bit	
		b'11	16 bit	

Addr 0x04: Soft Reset Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	RST

Name	Description	Value	Meaning	Ref.
RST	Soft Reset	**b'0**	Normal operation mode	
		b'1	Reset all function and return to '0' automatically thereafter	

Reserved Address 0x05

Addr 0x06: Master Clock Frequency Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	MCF			

Name	Description	Value	Meaning	Ref.
MCF	Master Clock Frequency	**b'0000**	3.072 MHz (WCK 48 kHz) / 2.8224 MHz (WCK 44.1 kHz)	
		b'0001	6.144 MHz (WCK 96 kHz)	
		b'0010	2.048 MHz (WCK 32 kHz)	

Addr 0x07: SRC Control0

Bit	7	6	5	4	3	2	1	0
Name	X	X	DCESW	X	FSFHM	FSFSM	X	X

Name	Description	Value	Meaning	Ref.
FSFSM	Frequency Stable Effect on Soft Mute	**b'0**	No effect on soft mute flag	
		b'1	Soft mute flag = 1 when unstable state	
FSFHM	Frequency Stable Effect on Hard Mute	b'0	No effect on hard mute flag	
		b'1	Hard mute flag = 1 when unstable state	
DCESW	DC Check Enable of SRC WCK	b'0	DC Check Disable in SRC WCK	
		b'1	DC Check Enable in SRC WCK	

Addr 0x08: SRC Control1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	FVT			

Name	Description	Value	Meaning	Ref.
FVT	Frequency variation threshold	b'0000 ~ b'1111	threshold value for frequency stable check (unsigned integer) default =**b'0111**	

Addr 0x09~0x0C: Mixer Gain

Bit	7	6	5	4	3	2	1	0
Name	X	MG						

Name	Description	Value	Meaning	Ref.
MG	Mixer gain	h'00 ~ h'7E	Mixer gain (refer to gain Table 14)	

$$\begin{bmatrix} mixer\_ch1\_output \\ mixer\_ch2\_output \end{bmatrix} = \begin{bmatrix} 0x09 & 0x0A \\ 0x0B & 0x0C \end{bmatrix} \bullet \begin{bmatrix} I2S\_ch1\_input \\ I2S\_ch2\_input \end{bmatrix}$$

Mixer equation

$$\begin{bmatrix} mixer\_ch1\_output \\ mixer\_ch2\_output \end{bmatrix} = \begin{bmatrix} 0dB(0x4E) & -\infty dB(0x00) \\ -\infty dB(0x00) & 0dB(0x4E) \end{bmatrix} \bullet \begin{bmatrix} I2S\_ch1\_input \\ I2S\_ch2\_input \end{bmatrix}$$

Reset default

Reserved Address 0x0D ~ 0x0F

Addr 0x10: Sampling Frequency for Audio Enhancement

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	FS_MM

Name	Description	Value	Meaning	Ref.
FS_MM	Sampling Frequency for Audio Enhancement	**b'0**	32 / 48 / 96 kHz	
		b'1	44.1 kHz	

Addr 0x11: Audio Enhancement Dialog Clarity Control0

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	EN

Name	Description	Value	Meaning	Ref.
EN	Dialog Clarity Enable	**b'0**	Disable	
		b'1	Enable	

Addr 0x12: Audio Enhancement Dialog Clarity Control1

Bit	7	6	5	4	3	2	1	0
Name	SIDE_GAIN				MID_GAIN			

Name	Description	Value	Meaning	Ref.
MID_GAIN	Center Gain	b'0000 ~ b'1100	-6dB ~ 6 dB Default = **b'0110 (0 dB)**	
SIDE_GAIN	Side Gain	b'0000 ~ b' 1100	-6dB ~ 6 dB Default = **b' 0110 (0 dB)**	

Addr 0x13: Audio Enhancement Dynamic Bass control

Bit	7	6	5	4	3	2	1	0
Name	EN	X	X	X	X	BOOST_GAIN		

Name	Description	Value	Meaning	Ref.
BOOST_GAIN	Boost Gain	b'000 ~ b'110	0 dB ~ 6 dB Default = **b'011 (3 dB)**	
EN	Dynamic Bass Enable	**b'0**		
		b'1	Enable	

Addr 0x14: Audio Enhancement Virtual Expander Control0

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	EN

Name	Description	Value	Meaning	Ref.
EN	Virtual Expander Enable	**b'0**	Disable	
		b'1	Enable	

0x15: Audio Enhancement Virtual Expander Control1

Bit	7	6	5	4	3	2	1	0
Name	SIDE_GAIN				MID_GAIN			

Name	Description	Value	Meaning	Ref.
MID_GAIN	Center Gain	b'0000 ~ b'1100	-6dB ~ 6 dB Default = **b'0110 (0 dB)**	
SIDE_GAIN	Side Gain	b'0000 ~ b' 1100	-6dB ~ 6 dB Default = **b' 0110 (0 dB)**	

0x16: Audio Enhancement Loudness Compensation Control

Bit	7	6	5	4	3	2	1	0
Name	EN	X	REF_DB					

Name	Description	Value	Meaning	Ref.
REF_DB	Reference dB	h'10 ~ h'28	-24 dB ~ 0 dB Default = **h'28 (0 dB)**	
EN	Loudness Compensation Enable	**b'0**	Disable	
		b'1	Enable	

Reserved Address 0x17 ~ 0x19

Addr 0x1A: Soft Volume Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	SVS	

Name	Description	Value	Meaning	Ref.
SVS	Soft volume speed	**b'00**	Medium speed	
		b'01	High speed	
		b'10	Low speed	
		b'11	soft volume change disabled	

Addr 0x1B: Auto Volume Sequence

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	EN

Name	Description	Value	Meaning	Ref.
EN	Auto Volume Sequence Enable	b'0	Disable	
		b'1	Enable MVOL = 0: mute → pwm off → pwm_mask low MVOL ≠ 0: pwm_mask high → pwm on → unmute	

Addr 0x1C: Master Volume

Bit	7	6	5	4	3	2	1	0
Name	MVOL							

Name	Description	Value	Meaning	Ref.
MVOL	Volume Control	b'00000000 ~ b'11111111	See master volume Table 12 Reset default is 0 (**0x00**) (= −∞ dB). 0xFF means 0dB with 0.5dB step	

Addr 0x1D: Master Volume Fine Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	MVFC	

Name	Description	Value	Meaning	Ref.
MVFC	Master Volume Fine Control	**b'00** ~ b'11	0dB ~ 0.375dB with 0.125dB step	

Addr 0x1E~0x1F: Ch1/2 Volume, respectively

Bit	7	6	5	4	3	2	1	0
Name	VOL							

Name	Description	Value	Meaning	Ref.
VOL	Volume Control	b'00000000 ~ b'11111111	See channel volume Table 13 Reset default is **0x9F** (= 0dB). 0xFF means 48dB with 0.5dB step.	

Addr 0x20~0x21: PEQ Filter Control0 for Ch1 and Ch2 respectively

Bit	7	6	5	4	3	2	1	0
Name	X	X	BQ3		BQ2		BQ1	

Name	Description	Value	Meaning	Ref.
BQ1	On/off Bi-Quad 1 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 1 of channel n	
		b'01	Enable Bi-Quad 1 of channel n	
		b'10	Enable Bi-Quad 1 as Loudness Filter	
BQ2	On/off Bi-Quad 2 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 2 of channel n	
		b'01	Enable Bi-Quad 2 of channel n	
		b'10	Enable Bi-Quad 2 as Loudness Filter	
BQ3	On/off Bi-Quad 3 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 3 of channel n	
		b'01	Enable Bi-Quad 3 of channel n	
		b'10	Enable Bi-Quad 3 as Loudness Filter	

Addr 0x22~0x23: PEQ Filter Control1 for Ch1 and Ch2 respectively

Bit	7	6	5	4	3	2	1	0
Name	X	BQ10	BQ9	BQ8	BQ7	BQ6	BQ5	BQ4

Name	Description	Value	Meaning	Ref.
BQ4	On/off Bi-Quad 4 of ch. n (n= 1,2)	**b'0**	Bypass Bi-Quad 4 of channel n	
		b'1	Enable Bi-Quad 4 of channel n	
BQ5	On/off Bi-Quad 5 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 5 of channel n	
		b'1	Enable Bi-Quad 5 of channel n	
BQ6	On/off Bi-Quad 6 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 6 of channel n	
		b'1	Enable Bi-Quad 6 of channel n	
BQ7	On/off Bi-Quad 7 of ch. n (n= 1,2)	**b'0**	Bypass Bi-Quad 7 of channel n	
		b'1	Enable Bi-Quad 7 of channel n	
BQ8	On/off Bi-Quad 8 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 8 of channel n	
		b'1	Enable Bi-Quad 8 of channel n	
BQ9	On/off Bi-Quad 9 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 9 of channel n	
		b'1	Enable Bi-Quad 9 of channel n	
BQ10	On/off Bi-Quad 10 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 10 of channel n	
		b'1	Enable Bi-Quad 10 of channel n	

Addr 0x24~0x25: PEQ Filter Control2 for Ch1 and Ch2 respectively

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	BQ14	BQ13	BQ12	BQ11

Name	Description	Value	Meaning	Ref.
BQ11	On/off Bi-Quad 11 of ch. n (n= 1,2)	**b'0**	Bypass Bi-Quad 11 of channel n	
		b'1	Enable Bi-Quad 11 of channel n	
BQ12	On/off Bi-Quad 12 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 12 of channel n	
		b'1	Enable Bi-Quad 12 of channel n	
BQ13	On/off Bi-Quad 13 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 13 of channel n	
		b'1	Enable Bi-Quad 13 of channel n	
BQ14	On/off Bi-Quad 14 of ch. n (n = 1,2)	**b'0**	Bypass Bi-Quad 14 of channel n	
		b'1	Enable Bi-Quad 14 of channel n	

Addr 0x26~0x27: PEQ Filter Control3 for Ch1 and Ch2 respectively

Bit	7	6	5	4	3	2	1	0
Name	BQ18		BQ17		BQ16		BQ15	

Name	Description	Value	Meaning	Ref.
BQ15	On/off Bi-Quad 15 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 15of channel n	
		b'01	Enable Bi-Quad 15 of channel n	
		b'10	Reserved	
		b'11	Reserved	
BQ16	On/off Bi-Quad 16 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 16 of channel n	
		b'01	Enable Bi-Quad 16 of channel n	
		b'10	Reserved	
		b'11	Reserved	
BQ17	On/off Bi-Quad 17 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 17 of channel n	
		b'01	Enable Bi-Quad 17 of channel n	
		b'10	Reserved	
		b'11	Reserved	
BQ18	On/off Bi-Quad 18 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 18 of channel n	
		b'01	Enable Bi-Quad 18 of channel n	
		b'10	Reserved	
		b'11	Reserved	

Addr 0x28~0x29: PEQ Filter Control4 for Ch1 and Ch2 respectively

Bit	7	6	5	4	3	2	1	0
Name	x	x	x	x	BQ20		BQ19	

Name	Description	Value	Meaning	Ref.
BQ19	On/off Bi-Quad 19 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 19 of channel n	
		b'01	Enable Bi-Quad19 of channel n	
		b'10	Reserved	
		b'11	Reserved	
BQ20	On/off Bi-Quad 20 of ch. n (n = 1,2)	**b'00**	Bypass Bi-Quad 20 of channel n	
		b'01	Enable Bi-Quad 20 of channel n	
		b'10	Reserved	
		b'11	Reserved	

Reserved Address 0x2A ~ 0x2D

Addr 0x2E: PEQ(BQ9 ~ BQ 14) Position Control for Ch1 and Ch2

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	P_SEL		

Name	Description	Value	Meaning	Ref.
P_SEL	Position Selection of BQ9 ~ BQ 14 of ch1/2	**b'000**	Before DRC	
		b'001	After DRC (BQ13 & 14)	
		b'010	After DRC (BQ11 & 12 & 13 & 14)	
		b'100	After DRC (BQ9 & 10 & 11 & 12 & 13 & 14)	

Reserved Address 0x2F ~ 0x3A

Addr 0x3B: DRC Control0

Bit	7	6	5	4	3	2	1	0
Name	CCO	X	X	X	X	2BM	SBM	CAS

Name	Description	Value	Meaning	Ref.
CAS	Coupled All pass Structure enable	**b'0**	Enable coupled all pass structure	
		b'1	Disable coupled all pass structure	
SBM	Sub band mode enable	**b'0**	Sub band mode Disable	
		b'1	Sub band mode Enable	
2BM	2band mode enable	**b'0**	1 band DRC	
		b'1	2 band DRC	
CCO	Clip control option	**b'0**	Clip off	
		b'1	Clip on	

Addr 0x3C: DRC Control1

Bit	7	6	5	4	3	2	1	0
Name	DE_L	X	X	X	X	X	X	X

Name	Description	Value	Meaning	Ref.
DE_L	DRC enable for Low band	**b'0**	Dynamic Range Compression off	
		b'1	Dynamic Range Compression on	

Reserved Address 0x3D

Addr 0x3E: DRC Control2

Bit	7	6	5	4	3	2	1	0
Name	DE_H	X	X	X	X	X	X	X

Name	Description	Value	Meaning	Ref.
DE_H	DRC enable for High band	**b'0**	Dynamic Range Compression off	
		b'1	Dynamic Range Compression on	

Reserved Address 0x3F

Addr 0x40: DRC Control3

Bit	7	6	5	4	3	2	1	0
Name	DE_S	X	X	X	X	X	X	X

Name	Description	Value	Meaning	Ref.
DE_S	DRC enable for Sub band	**b'0**	Dynamic Range Compression off	
		b'1	Dynamic Range Compression on	

Reserved Address 0x41

Addr 0x42: Limiter Control

Bit	7	6	5	4	3	2	1	0
Name	LM_EN	X	X	X	X	X	X	X

Name	Description	Value	Meaning	Ref.
LM_EN	Limiter enable	**b'0**	Limiter off	
		b'1	Limiter on	

Reserved Address: 0x43 ~ 0x4F

Addr 0x50: Threshold Table Mapping Coefficient for DRC

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	COEF_SEL				

Name	Description	Value	Meaning	Ref.
COEF_SEL	Threshold Table Mapping	**d'10**	Default Value: 10 (= 2.0) The range is between 0 and 20	

Reserved Address: 0x51 ~ 0x5A

Addr0x5B: AccDRC & Limiter Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	LM_SEL	S_SEL	H_SEL	L_SEL

Name	Description	Value	Meaning	Ref.
L_SEL	RMS Calculation Type of Low-Band	**b'0**	RMS	
		b'1	Envelope	
H_SEL	RMS Calculation Type of High-Band	**b'0**	RMS	
		b'1	Envelope	
S_SEL	RMS Calculation Type of Sub-Band	**b'0**	RMS	
		b'1	Envelope	
LM_SEL	RMS Calculation Type of Limiter	**b'0**	RMS	
		b'1	Envelope	

Addr 0x5C: AccDRC Release Delay Control0

Bit	7	6	5	4	3	2	1	0
Name	R_DELAY_L							

Name	Description	Value	Meaning	Ref.
R_DELAY_L	Release Delay of Low Band	d0 ~ **d150**	Each step is 16.	

Addr 0x5D: AccDRC Release Delay Control1

Bit	7	6	5	4	3	2	1	0
Name	R_DELAY_H							

Name	Description	Value	Meaning	Ref.
R_DELAY_H	Release Delay of High Band	d0 ~ **d150**	Each step is 16.	

Addr 0x5E: AccDRC Release Delay Control2

Bit	7	6	5	4	3	2	1	0
Name	R_DELAY_S							

Name	Description	Value	Meaning	Ref.
R_DELAY_S	Release Delay of Sub Band	d0 ~ **d150**	Each step is 16.	

Addr 0x5F: Limiter Recover Delay Control

Bit	7	6	5	4	3	2	1	0
Name	R_DELAY_LM							

Name	Description	Value	Meaning	Ref.
R_DELAY_LM	Recover Delay of Limiter	d0 ~ **d150**	Each step is 16.	

Addr 0x60: DRC Delay Line Control0

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	DLL				

Name	Description	Value	Meaning	Ref.
DLL	Delay line length (L & H & S)	b'00000~ **b'10100**	Delay line length. 0~20(decimal)	

Addr 0x61: Limiter Delay Line Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	DLL_LM				

Name	Description	Value	Meaning	Ref.
DLL_LM	Delay Line Length of Limiter	b'00000~ **b'10100**	Delay line length. 0~20(decimal)	

Reserved Address: 0x62 ~ 0x69

Addr 0x6A: Soft Mute Control

Bit	7	6	5	4	3	2	1	0
Name	SMCS	X	X	X	X	X	SM2	SM1

Name	Description	Value	Meaning	Ref.
SMn	Softmute	b'0	unmute	
		b'1	mute	
SMCS	Soft Mute Change speed	**b'0**	42/46 msec(at 96/88.2kHz))	
		b'1	Hard change	

Addr 0x6B: Auto-Mute Control for Ch1 & Ch2

Bit	7	6	5	4	3	2	1	0
Name	X	EAMC	ART		ADT			

Name	Description	Value	Meaning	Ref.
ADT	Auto-mute detection threshold	**b'0000** ~ b'1111	Unsigned integer between 0 and 15 Refer to Auto Mute detection threshold Table 15 for threshold values.	
ART	Auto-mute response time	**b'00**	5 msec	
		b'01	50 msec	
		b'10	500 msec	
		b'11	2 sec	
EAMC	Effect of Auto-mute condition	**b'0**	Auto mute disable(No-Effect)	
		b'1	Stop PWM switching when auto-mute condition is met.	

Addr 0x6C: Ch1&Ch2 Prescaler Value Control

Bit	7	6	5	4	3	2	1	0
Name	PS_LR							

Name	Description	Value	Meaning	Ref.
PS_LR	Prescaler value	b'00000000 ~ b'11111111	default = **0x4C**	

Addr 0x6D: NS Soft Mute Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	TIME_LIM	ENABLE	CNT_THR			

Name	Description	Value	Meaning	Ref.
CNT_THR	Minimum Counting Value	b'0000~ b'1111	Minimum counting value of continuous zeros for forcing NS_OUT as 0. default = **b'0110**	
ENABLE	NS Soft Mute Enable	**b'0**	Disable	
		b'1	Enable	
TIME_LIM	Time Limit on Finding Continuous Zeros	**b'0**	Time Limit = 200ms	
		b'1	Time Limit = 400ms	

Addr 0x6E: Modulation Index & NS-Type Control

Bit	7	6	5	4	3	2	1	0
Name	D_POS			FB	X	NTF_ORDER	MPW	

Name	Description	Value	Meaning	Ref.
MPW	Minimum Pulse Width for Ch 1&2	b'00	Minimum pulse width = 80 ns	
		b'01	Minimum pulse width = 60 ns	
		b'10	Minimum pulse width = 40 ns	
		b'11	Minimum pulse width = 20 ns	
NTF_ORDER	NTF Order Select	**b'0**	NTF Order = 4	
		b'1	NTF Order = 5	
FB	Feed Back On/off	b'0	NS Feed Back off	
		b'1	NS Feed Back on	
D_POS	Dither Position Selector	**b'000**	No left shift on dither value = Dither off	
		b'001	1bit left shift on dither value	
		b'010	2bit left shift on dither value	
		b'011	3bit left shift on dither value	
		b'100	4bit left shift on dither value	
		b'101	5bit left shift on dither value	
		b'110	6bit left shift on dither value	
		b'111	7bit left shift on dither value	

Addr 0x6F: NS Feedback Limit

Bit	7	6	5	4	3	2	1	0
Name	X	FBMAX						

Name	Description	Value	Meaning	Ref.
FBMAX	Feedback on/off	b'0000000 ~b'1111111	Feedback limit, default = **0x04**	

Reserved Address: 0x70 ~ 0x74

Addr 0x75: PWM_MASK Control0

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	FD	FPMLD	PWMM	

Name	Description	Value	Meaning	Ref.
PWMM	PWM MASK Control	**b'10**	PWM MASK output is low.	
		Otherwise	PWM MASK output is high.	
FPMLD	Permanent Low Disable	**b'0**	No effect	
		b'1	Reset the Auto PWM_MASK restore counter to 0	
FD	FAULT Disable	**b'0**	FAULT is effective for Protection	
		b'1	FAULT is ineffective for Protection	

Addr 0x76: PWM_MASK Control1

Bit	7	6	5	4	3	2	1	0
Name	PWMM_RIC		PWMM_RCT			PWMM_HT		

Name	Description	Value	Meaning	Ref.
PWMM_HT	PWM_MASK Low Hold Time	b'000	0.5 msec Hold Time	
		b'001	1 msec Hold Time	
		b'010	2 msec Hold Time	
		b'011	4 msec Hold Time	
		b'100	8 msec Hold Time	
		b'101	16msec Hold Time	
PWMM_RCT	PWM_MASK Auto Restore Counter Threshold	b'000	2	
		b'001	5	
		b'010	10	
		b'011	15	
		b'100	20	
		b'101	25	
		b'110	30	
		b'111	Infinity	
PWMM_RIC	PWM_MASK Auto Restore Interval Ratio Control	**b'00**	2	
		b'01	4	
		b'11	0	

Addr 0x77: PWM_MASK Control2

Bit	7	6	5	4	3	2	1	0
Name	SHE	POE	X	X	X	HT2		

Name	Description	Value	Meaning	Ref.
HT2	Hold Time 2 apply start point (restore counter)	b'000	100 msec Hold Time	
		b'001	200 msec Hold Time	
		b'010	400 msec Hold Time	
		b'011	600 msec Hold Time	
		b'100	800 msec Hold Time	
		b'101	1 sec Hold Time	
		b'110	2 sec Hold Time	
		b'111	4 sec Hold Time	
POE	PWM off when PWM_MASK off and PWM on when PWM_MASK recovers	b'0	Disable	
		b'1	Enable	
SHE	Second Hold time Enable	**b'0**	Disable	
		b'1	Enable	

Addr 0x78: PWM_MASK Control3

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	PMMC	POC

Name	Description	Value	Meaning	Ref.
POC	PWM Off Control	**b'0**	Even if Auto PWM_MASK condition is met, the PWM output of all channels is not affected.	
		b'1	When Auto PWM_MASK condition is met, the PWM output of all channels goes to the defined state which is set by the PWM off state control registers.	
PMMC	PWM_MASK Control	**b'0**	Even if Auto PWM_MASK condition is met, the PWM_MASK is not affected.	
		b'1	When Auto PWM_MASK condition is met, the PWM_MASK output goes to Low state.	

Addr 0x79: PWM_MASK Control4

Bit	7	6	5	4	3	2	1	0
Name	X	VMSK2	VMSK1	VMSK0	X	PMSK2	PMSK1	PMSK0

Name	Description	Value	Meaning	Ref.
PMSKn	Masking bit of PWM off control	**b'0**	Mask bit indicating the validity of n-th bit of Addr 0xA2 system register: If the n-th bit of this register is zero, the n-th bit of Addr 0xA2 system register is invalid. The n-th bit of Addr 0xA2 is valid only when the n-th mask bit is one.	
		b'1		
VMSKn	Masking bit of PWM_MASK signal	**b'0**		
		b'1		

Addr 0x7A: PWM_MASK Control5

Bit	7	6	5	4	3	2	1	0
Name	VMSK3	VMSK2	VMSK1	VMSK0	PMSK3	PMSK2	PMSK1	PMSK0

Name	Description	Value	Meaning	Ref.
PMSKn	Masking bit of PWM off control	**b'0**	Mask bit indicating the validity of n-th bit of Addr 0xA1 system register: If the n-th bit of this register is zero, the n-th bit of Addr 0xA1 system register is invalid. The n-th bit of Addr 0xA1 is valid only when the n-th mask bit is one.	
		b'1		
VMSKn	Masking bit of PWM_MASK signal	**b'0**		

Addr 0x7B: PWM Switching On/Off Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	PON2	PON1

Name	Description	Value	Meaning	Ref.
PONn	Switching output On/off control	b'0	Channel n PWM switching on	
		b'1	Channel n PWM switching off	

Reserved Address: 0x7C ~ 0x7D

Addr 0x7E: Bi-Quad Filter Coefficient Page

Bit	7	6	5	4	3	2	1	0
	COEFF_P							

Name	Description	Value	Meaning	Ref.
	Coefficient Write Enable	**h'00**	Disable coefficient write	
		h'81	Coefficient Write Enable for CH1 PEQs	
		h'82	Coefficient Write Enable for CH2 PEQs	
		h'86, h'87	Coefficient Write Enable for DRC & Limiter	
		h'B0	Coefficient Write Enable for Dialog Clarity Parameters	
		h'B1	Coefficient Write Enable for Dynamic Bass Parameters	
		h'B2	Coefficient Write Enable for Virtual Expander Parameters	
		h'B3	Coefficient Write Enable for Audio Enhancement Loudness Parameters	
		h'B8	Coefficient Write Enable for Dialog Clarity Parameters (44.1KHz)	
		h'B9	Coefficient Write Enable for Dynamic Bass Parameters (44.1KHz)	
		h'BA	Coefficient Write Enable for Virtual Expander Parameters (44.1KHz)	
		h'BB	Coefficient Write Enable for Audio Enhancement Loudness Parameters (44.1KHz)	

Note: When writing into BQ1~BQ11 coefficients, Should write for both ch1 and ch2separately.

When writing into BQ12~BQ20 coefficients, Just write for ch1.

(BQ12~BQ20 coefficients are same for both CH1 and CH2)

Reserved Address: 0x7F ~ 0x83

Addr 0x84: PWM Phase Control

Bit	7	6	5	4	3	2	1	0
Name	PPC				PFC			

Name	Description	Value	Meaning	Ref.
PFC	PWM phase Fine Control	**b'0000** ~ b'1001	Range is 0°~14.94° with 1.66° step	In Single ended mode, fixed as PFC = b'0000, and PPC = b'0110 (90°)
PPC	PWM Phase Control	b'0000 ~ b'1100	Range is 0°~180° with 15°step. default =**b'0110** (90°)	

Addr 0x85: Miscellaneous PWM Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	BHL	AHL	MD	

Name	Description	Value	Meaning	Ref.
MD	PWM Output Mode	b'00	AD mode	
		b'10	BD mode	
		others	Reserved	
AHL	A-Out State When Switching Off	**b'0**	Low	
		b'1	High	
BHL	B-Out State When Switching Off	**b'0**	Low	
		b'1	High	

Addr 0x86: PWM BD Mode Control0

Bit	7	6	5	4	3	2	1	0
Name	X	BOW						

Name	Description	Value	Meaning	Ref.
BOW	BD Offset Width	**h'0E**	Unsigned 0~64	

Reserved Address: 0x87 ~ 0x8D

Addr 0x8E: PWM Output Port Control for PWM Port 1A & 1B

Bit	7	6	5	4	3	2	1	0
Name	X	X	OPM1B			OPM1A		

Name	Description	Value	Meaning	Ref.
OPM1A	Select source channel for PWM output port 1A	**000**	PWM1A is connected to PWM port 1A	
		001	PWM1B is connected to PWM port 1A	
		010	PWM2A is connected to PWM port 1A	
		011	PWM2B is connected to PWM port 1A	
OPM1B	Select source channel for PWM output port 1B	000	PWM1A is connected to PWM port 1B	
		001	PWM1B is connected to PWM port 1B	
		010	PWM2A is connected to PWM port 1B	
		011	PWM2B is connected to PWM port 1B	

Addr 0x8F: PWM Output Port Control for PWM Port 2A & 2B

Bit	7	6	5	4	3	2	1	0
Name	X	X	OPM2B			OPM2A		

Name	Description	Value	Meaning	Ref.
OPM2A	Select source channel for PWM output port 2A	000	PWM1A is connected to PWM port 2A	
		001	PWM1B is connected to PWM port 2A	
		010	PWM2A is connected to PWM port 2A	
		011	PWM2B is connected to PWM port 2A	
OPM2B	Select source channel for PWM output port 2B	000	PWM1A is connected to PWM port 2B	
		001	PWM1B is connected to PWM port 2B	
		010	PWM2A is connected to PWM port 2B	
		011	PWM2B is connected to PWM port 2B	

Addr 0x90: Soft Start Control0

Bit	7	6	5	4	3	2	1	0
Name	PSE	SRT						

Name	Description	Value	Meaning	Ref.
SRT	Step Repeat Time	h'00 ~ h'7F	Repeat time of each step (default = **h'10** – means repeat 17 times)	
PSE	PWM Soft Start Enable	b'0	Disable	
		b'1	Enable (only under AD mode)	

Addr 0x91: Soft Start Control1

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	S_MPW	

Name	Description	Value	Meaning	Ref.
S_MPW	Soft Start Minimum Pulse Width	b'00	First pulse width = 20 ns	
		b'01	First pulse width = 40 ns	
		b'10	First pulse width = 60 ns	
		b'11	First pulse width = 80 ns	

Reserved Address: 0x92

Addr 0x93: AD DC Protection Control0

Bit	7	6	5	4	3	2	1	0
Name	PDH				PDL			

Name	Description	Value	Meaning	Ref.
PDL	PWM Duty Low for Modulation Index Error	b'0000	40%	
		b'0001	35%	
		b'0010	30%	
		b'0011	25%	
		b'0100	20%	
		b'0101	15%	
		b'0110	10%	
		b'0111	5%	
		b'1000	45%	
PDH	PWM Duty High for Modulation Index Error	b'0000	60%	
		b'0001	65%	
		b'0010	70%	
		b'0011	75%	
		b'0100	80%	
		b'0101	85%	
		b'0110	90%	
		b'0111	95%	
		b'1000	55%	

Addr 0x94: BD **DC Protection Control1**

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	BDHMI			

Name	Description	Value	Meaning	Ref.
BDHMI	BD Duty High for Modulation Index Error	**b'0000**	5%	
		b'0001	10%	
		b'0010	15%	
		b'0011	20%	
		b'0100	25%	
		b'0101	30%	
		b'0110	35%	
		b'0111	40%	
		b'1000	45%	
		b'1001	50%	

Reserved Address: 0x95 ~ 0x98

Addr 0x99: Watch Dog Control0

Bit	7	6	5	4	3	2	1	0
Name	RT							

Name	Description	Value	Meaning	Ref.
RT	Release Time	h'00 ~ h'FF	WDE becomes 0 if Watch Dog detects no error during RT*10msec after WDE has been occurred. default = **0x10**	

Addr 0x9A: Watch Dog Control1

Bit	7	6	5	4	3	2	1	0
Name	ULM[15:8]							

Name	Description	Value	Meaning	Ref.
ULM	Upper Limit MSB	h'00 ~ h'FF	Upper limit on ratio of BCK to CLK_FR_4 default = **0x00**	

Addr 0x9B: Watch Dog Control2

Bit	7	6	5	4	3	2	1	0
Name	ULM[7:0]							

Name	Description	Value	Meaning	Ref.
ULM	Upper Limit LSB	h'00 ~ h'FF	Upper limit on ratio of BCK to CLK_FR_4 default = **0x20**	

Addr 0x9C: Watch Dog Control3

Bit	7	6	5	4	3	2	1	0
Name	LLM[3:0]				0	0	0	WON

Name	Description	Value	Meaning	Ref.
LLM	Lower Limit	b'0000 ~ b'1111	Lower limit on ratio of BCK to CLK_FR_4 **default = b'1001**	
WON	Watch-Dog On	b'0	OFF	
		b'1	ON	

Reserved Address: 0x9D

Addr 0x9E: DC Protection Control2

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	PCE_EN	DCE_EN	MIE_EN

Name	Description	Value	Meaning	Ref.
MIE_EN	Modulation Index Error Check Enable	**b'0**	Modulation Index Error Check Disable	
		b'1	Modulation Index Error Check Enable	
DCE_EN	DRC Coefficient Error Check Enable	**b'0**	DRC Coefficient Error Check Disable	
		b'1	DRC Coefficient Error Check Enable	
PCE_EN	PEQ Coefficient Error Check Enable	**b'0**	PEQ Coefficient Error Check Disable	
		b'1	PBQ Coefficient Error Check Enable	

Addr 0x9F: DC Protection Error Status (read only)

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	PCE	DCE	MIE

Name	Description	Value	Meaning	Ref.
MIE	Modulation Index Error	**b'0**		
		b'1	Modulation Index Error	
DCE	DRC Coefficient Error	**b'0**		
		b'1	DRC Coefficient Error	
PCE	PEQ Coefficient Error	**b'0**		
		b'1	PEQ Coefficient Error	

Addr 0xA0: System Status Register (0xA1, 0xA2) Holding Control1

Bit	7	6	5	4	3	2	1	0
Name	HIWK	HIBK	HWDE	X	HMEF	HMPW	HULCK	X

Name	Description	Value	Meaning	Ref.
HULCK	Enable Bit of Holding the ULCK status	**b'0**	Update the new value without holding the ULCK status bit of 0xA2	
		b'1	Hold the first different value	
HMPW	Enable Bit of Holding the MPW status	**b'0**	Update the new value without holding the MPW status bit of 0xA2	
		b'1	Hold the first different value	
HMEF	Enable Bit of Holding the MEF status	**b'0**	Update the new value without holding the MEF status bit of 0xA1	
		b'1	Hold the first different value	
HWDE	Enable Bit of Holding the WDE status	**b'0**	Update the new value without holding the WDE status bit of 0xA1	
		b'1	Hold the first different value	
HIBK	Enable Bit of Holding the IBK status	**b'0**	Update the new value without holding the IBK status bit of 0xA1	
		b'1	Hold the first different value	
HIWK	Enable Bit of Holding the IWK status	**b'0**	Update the new value without holding the IWK status bit of 0xA1	
		b'1	Hold the first different value	

Addr 0xA1: Watch Dog Error Status (read only)

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	MIE	IWK	IBK	WDE

Name	Description	Value	Meaning	Ref.
WDE	Watch Dog Ratio Error	b'0		
		b'1	Watch Dog Error	
IBK	IIS BCK Ratio Error	b'0		
		b'1	IIS BCK Ratio Error	
IWK	IIS WCK Ratio Error	b'0		
		b'1	IIS WCK Ratio Error	
MIE	Modulation Index Error	**b'0**		
		b'1	Modulation Index Error	

Addr 0xA2: System Error Status (read only)

Bit	7	6	5	4	3	2	1	0
Name	FSI		PSB	PDM		MPW	ULCK	PPM

Name	Description	Value	Meaning	Ref.
PPM	Permanent PWMMASK Indication flag	b'0		
		b'1	Indicated that PWM_MASK is in Permanent LOW state	
ULCK	Sampled PLL Unlock error	b'0	PLL is locked state.	
		b'1	PLL is unlocked state.	
MPW	MCK/WCK Ratio error	b'0	Ratio is incorrect.	
		b'1	Ratio is correct.	
PDM	Power Die Monitor (Temperature, Current, Voltage, Protection Error)	b'00	Current protection error	
		b'01	Voltage protection error	
		b'10	Temperature protection error	
		b'11	Normal state	
PSB	PWM switching on/off State Bit	b'0	PWM switching off state	
		b'1	PWM switching on state	
FSI	Sampling Frequency Information	b'00	48 kHz (44.1kHz)	
		b'01	96 kHz	
		b'10	32 kHz	

Reserved Address: 0xA3 ~ 0xA6

Addr 0xA7: Power Meter Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	PM_POS	X	X	PM_CH	

Name	Description	Value	Meaning	Ref.
PM_CH	Power Meter Detect Channel	**b'00**	L+R (default)	
		b'01	L channel	
		b'10	R channel	
PM_POS	Power meter Detect Position	**b'0**	After volume (default)	
		b'1	Before volume (from digital input)	

Addr 0xA8: Power Meter (read only)

Bit	7	6	5	4	3	2	1	0
Name	Value of Power Meter							

Reserved Address: 0xA9

Addr 0xAA: WCK Synchronization Control

Bit	7	6	5	4	3	2	1	0
Name	SYN_EN	X	X	X	X	X	X	X

Name	Description	Value	Meaning	Ref.
SYN_EN	WCK Synchronization	**b'0**	Disable	
		b'1	Enable	

Reserved Address: 0xAB

Addr 0xAC: Driver Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	SHDN

Name	Description	Value	Meaning	Ref.
SHDN	Shutdown	b'0	Set SHDN pin as low	
		b'1	Set SHDN pin as high	

Addr 0xAD: IIS Sdata_Out Control

Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	OUT_SEL

Name	Description	Value	Meaning	Ref.
OUT_SEL	Select Data for I^2S OUT	**b'0**	Data after soft mute stage is selected	
		b'1	Data before EQ stage is selected	

Addr 0xAE: I^2C Glitch filter

Bit	7	6	5	4	3	2	1	0
Name	GFE	GW						

Name	Description	Value	Meaning	Ref.
GW	Glitch Width	h'00 ~ h'7F	Minimum pulse width = GW + 20 ns Reset default = 15 * 10 ns (default = **h'0F**)	
GFE	Glitch Filter Enable	**b'0**	Glitch filter enable	
		b'1	Glitch filter disable	

Reserved Address: 0xAF ~ B0

Addr 0xB1: Monitor

Bit	7	6	5	4	3	2	1	0
Name	Monitor2				Monitor1			

Name	Description	Value	Meaning	Ref.
Monitor1	This output doesn't come from Power Device.	b'0000	Reserved	
		b'0001	Pwm1a=> MONITOR_1 pin	
		b'0010	Pwm1b => MONITOR_1 pin	
		b'0011	pwm2a => MONITOR_1 pin	
		b'0100	Pwm2b => MONITOR_1 pin	
		b'1111	SDATA out => MONITOR_1 pin	
Monitor2	This output doesn't come from Power Device.	b'0000	Reserved	
		b'0001	Pwm1a=> MONITOR_2 pin	
		b'0010	Pwm1b => MONITOR_2 pin	
		b'0011	pwm2a => MONITOR_2 pin	
		b'0100	Pwm2b => MONITOR_2 pin	
		b'1111	SDATA out => MONITOR_2 pin	

Reserved Address 0xB2 ~ 0xFF

B. Configuration Register Value Reference

Table 12. Master Volume

Index	dB	Index	dB	Index	dB	Index	dB	Index	dB	Index	dB
0xFF	0.0	0xD4	-21.5	0xA9	-43.0	0x7E	-64.5	0x53	-86.0	0x28	-107.5
0xFE	-0.5	0xD3	-22.0	0xA8	-43.5	0x7D	-65.0	0x52	-86.5	0x27	-108.0
0xFD	-1.0	0xD2	-22.5	0xA7	-44.0	0x7C	-65.5	0x51	-87.0	0x26	-108.5
0xFC	-1.5	0xD1	-23.0	0xA6	-44.5	0x7B	-66.0	0x50	-87.5	0x25	-109.0
0xFB	-2.0	0xD0	-23.5	0xA5	-45.0	0x7A	-66.5	0x4F	-88.0	0x24	-109.5
0xFA	-2.5	0xCF	-24.0	0xA4	-45.5	0x79	-67.0	0x4E	-88.5	0x23	-110.0
0xF9	-3.0	0xCE	-24.5	0xA3	-46.0	0x78	-67.5	0x4D	-89.0	0x22	-110.5
0xF8	-3.5	0xCD	-25.0	0xA2	-46.5	0x77	-68.0	0x4C	-89.5	0x21	-111.0
0xF7	-4.0	0xCC	-25.5	0xA1	-47.0	0x76	-68.5	0x4B	-90.0	0x20	-111.5
0xF6	-4.5	0xCB	-26.0	0xA0	-47.5	0x75	-69.0	0x4A	-90.5	0x1F	-112.0
0xF5	-5.0	0xCA	-26.5	0x9F	-48.0	0x74	-69.5	0x49	-91.0	0x1E	-112.5
0xF4	-5.5	0xC9	-27.0	0x9E	-48.5	0x73	-70.0	0x48	-91.5	0x1D	-113.0
0xF3	-6.0	0xC8	-27.5	0x9D	-49.0	0x72	-70.5	0x47	-92.0	0x1C	-113.5
0xF2	-6.5	0xC7	-28.0	0x9C	-49.5	0x71	-71.0	0x46	-92.5	0x1B	-114.0
0xF1	-7.0	0xC6	-28.5	0x9B	-50.0	0x70	-71.5	0x45	-93.0	0x1A	-114.5
0xF0	-7.5	0xC5	-29.0	0x9A	-50.5	0x6F	-72.0	0x44	-93.5	0x19	-115.0
0xEF	-8.0	0xC4	-29.5	0x99	-51.0	0x6E	-72.5	0x43	-94.0	0x18	-115.5
0xEE	-8.5	0xC3	-30.0	0x98	-51.5	0x6D	-73.0	0x42	-94.5	0x17	-116.0
0xED	-9.0	0xC2	-30.5	0x97	-52.0	0x6C	-73.5	0x41	-95.0	0x16	-116.5
0xEC	-9.5	0xC1	-31.0	0x96	-52.5	0x6B	-74.0	0x40	-95.5	0x15	-117.0
0xEB	-10.0	0xC0	-31.5	0x95	-53.0	0x6A	-74.5	0X3F	-96.0	0x14	-117.5
0xEA	-10.5	0xBF	-32.0	0x94	-53.5	0x69	-75.0	0X3E	-96.5	0x13	-118.0
0xE9	-11.0	0xBE	-32.5	0x93	-54.0	0x68	-75.5	0X3D	-97.0	0x12	-118.5
0xE8	-11.5	0xBD	-33.0	0x92	-54.5	0x67	-76.0	0X3C	-97.5	0x11	-119.0
0xE7	-12.0	0xBC	-33.5	0x91	-55.0	0x66	-76.5	0X3B	-98.0	0x10	-119.5
0xE6	-12.5	0xBB	-34.0	0x90	-55.5	0x65	-77.0	0X3A	-98.5	0x0F	-120.0
0xE5	-13.0	0xBA	-34.5	0x8F	-56.0	0x64	-77.5	0X39	-99.0	0x0E	-120.5
0xE4	-13.5	0xB9	-35.0	0x8E	-56.5	0x63	-78.0	0X38	-99.5	0x0D	-121.0
0xE3	-14.0	0xB8	-35.5	0x8D	-57.0	0x62	-78.5	0X37	-100.0	0x0C	-121.5
0xE2	-14.5	0xB7	-36.0	0x8C	-57.5	0x61	-79.0	0X36	-100.5	0x0B	-122.0
0xE1	-15.0	0xB6	-36.5	0x8B	-58.0	0x60	-79.5	0X35	-101.0	0x0A	-122.5
0xE0	-15.5	0xB5	-37.0	0x8A	-58.5	0x5F	-80.0	0X34	-101.5	0x09	-123.0
0xDF	-16.0	0xB4	-37.5	0x89	-59.0	0x5E	-80.5	0X33	-102.0	0x08	-123.5
0xDE	-16.5	0xB3	-38.0	0x88	-59.5	0x5D	-81.0	0X32	-102.5	0x07	-124.0
0xDD	-17.0	0xB2	-38.5	0x87	-60.0	0x5C	-81.5	0X31	-103.0	0x06	-124.5
0xDC	-17.5	0xB1	-39.0	0x86	-60.5	0x5B	-82.0	0X30	-103.5	0x05	-125.0
0xDB	-18.0	0xB0	-39.5	0x85	-61.0	0x5A	-82.5	0x2F	-104.0	0x04	-125.5
0xDA	-18.5	0xAF	-40.0	0x84	-61.5	0x59	-83.0	0x2E	-104.5	0x03	-∞
0xD9	-19.0	0xAE	-40.5	0x83	-62.0	0x58	-83.5	0x2D	-105.0	0x02	-∞
0xD8	-19.5	0xAD	-41.0	0x82	-62.5	0x57	-84.0	0x2C	-105.5	0x01	-∞
0xD7	-20.0	0xAC	-41.5	0x81	-63.0	0x56	-84.5	0x2B	-106.0	0x00	-∞
0xD6	-20.5	0xAB	-42.0	0x80	-63.5	0x55	-85.0	0x2A	-106.5		
0xD5	-21.0	0xAA	-42.5	0x7F	-64.0	0x54	-85.5	0x29	-107.0		

Table 13. Channel Volume

Index	dB	Index	dB	Index	dB	Index	dB	Index	dB	Index	dB
0xFF	48.0	0xD4	26.5	0xA9	5.0	0x7E	-16.5	0x53	-38.0	0x28	-59.5
0xFE	47.5	0xD3	26.0	0xA8	4.5	0x7D	-17.0	0x52	-38.5	0x27	-60.0
0xFD	47.0	0xD2	25.5	0xA7	4.0	0x7C	-17.5	0x51	-39.0	0x26	-60.5
0xFC	46.5	0xD1	25.0	0xA6	3.5	0x7B	-18.0	0x50	-39.5	0x25	-61.0
0xFB	46.0	0xD0	24.5	0xA5	3.0	0x7A	-18.5	0x4F	-40.0	0x24	-61.5
0xFA	45.5	0xCF	24.0	0xA4	2.5	0x79	-19.0	0x4E	-40.5	0x23	-62.0
0xF9	45.0	0xCE	23.5	0xA3	2.0	0x78	-19.5	0x4D	-41.0	0x22	-62.5
0xF8	44.5	0xCD	23.0	0xA2	1.5	0x77	-20.0	0x4C	-41.5	0x21	-63.0
0xF7	44.0	0xCC	22.5	0xA1	1.0	0x76	-20.5	0x4B	-42.0	0x20	-63.5
0xF6	43.5	0xCB	22.0	0xA0	0.5	0x75	-21.0	0x4A	-42.5	0x1F	-64.0
0xF5	43.0	0xCA	21.5	0x9F	0.0	0x74	-21.5	0x49	-43.0	0x1E	-64.5
0xF4	42.5	0xC9	21.0	0x9E	-0.5	0x73	-22.0	0x48	-43.5	0x1D	-65.0
0xF3	42.0	0xC8	20.5	0x9D	-1.0	0x72	-22.5	0x47	-44.0	0x1C	-65.5
0xF2	41.5	0xC7	20.0	0x9C	-1.5	0x71	-23.0	0x46	-44.5	0x1B	-66.0
0xF1	41.0	0xC6	19.5	0x9B	-2.0	0x70	-23.5	0x45	-45.0	0x1A	-66.5
0xF0	40.5	0xC5	19.0	0x9A	-2.5	0x6F	-24.0	0x44	-45.5	0x19	-67.0
0xEF	40.0	0xC4	18.5	0x99	-3.0	0x6E	-24.5	0x43	-46.0	0x18	-67.5
0xEE	39.5	0xC3	18.0	0x98	-3.5	0x6D	-25.0	0x42	-46.5	0x17	-68.0
0xED	39.0	0xC2	17.5	0x97	-4.0	0x6C	-25.5	0x41	-47.0	0x16	-68.5
0xEC	38.5	0xC1	17.0	0x96	-4.5	0x6B	-26.0	0x40	-47.5	0x15	-69.0
0xEB	38.0	0xC0	16.5	0x95	-5.0	0x6A	-26.5	0X3F	-48.0	0x14	-69.5
0xEA	37.5	0xBF	16.0	0x94	-5.5	0x69	-27.0	0X3E	-48.5	0x13	-70.0
0xE9	37.0	0xBE	15.5	0x93	-6.0	0x68	-27.5	0X3D	-49.0	0x12	-70.5
0xE8	36.5	0xBD	15.0	0x92	-6.5	0x67	-28.0	0X3C	-49.5	0x11	-71.0
0xE7	36.0	0xBC	14.5	0x91	-7.0	0x66	-28.5	0X3B	-50.0	0x10	-71.5
0xE6	35.5	0xBB	14.0	0x90	-7.5	0x65	-29.0	0X3A	-50.5	0x0F	-72.0
0xE5	35.0	0xBA	13.5	0x8F	-8.0	0x64	-29.5	0X39	-51.0	0x0E	-72.5
0xE4	34.5	0xB9	13.0	0x8E	-8.5	0x63	-30.0	0X38	-51.5	0x0D	-73.0
0xE3	34.0	0xB8	12.5	0x8D	-9.0	0x62	-30.5	0X37	-52.0	0x0C	-73.5
0xE2	33.5	0xB7	12.0	0x8C	-9.5	0x61	-31.0	0X36	-52.5	0x0B	-74.0
0xE1	33.0	0xB6	11.5	0x8B	-10.0	0x60	-31.5	0X35	-53.0	0x0A	-74.5
0xE0	32.5	0xB5	11.0	0x8A	-10.5	0x5F	-32.0	0X34	-53.5	0x09	-75.0
0xDF	32.0	0xB4	10.5	0x89	-11.0	0x5E	-32.5	0X33	-54.0	0x08	-75.5
0xDE	31.5	0xB3	10.0	0x88	-11.5	0x5D	-33.0	0X32	-54.5	0x07	-76.0
0xDD	31.0	0xB2	9.5	0x87	-12.0	0x5C	-33.5	0X31	-55.0	0x06	-76.5
0xDC	30.5	0xB1	9.0	0x86	-12.5	0x5B	-34.0	0X30	-55.5	0x05	-77.0
0xDB	30.0	0xB0	8.5	0x85	-13.0	0x5A	-34.5	0x2F	-56.0	0x04	-77.5
0xDA	29.5	0xAF	8.0	0x84	-13.5	0x59	-35.0	0x2E	-56.5	0x03	-78.0
0xD9	29.0	0xAE	7.5	0x83	-14.0	0x58	-35.5	0x2D	-57.0	0x02	-78.5
0xD8	28.5	0xAD	7.0	0x82	-14.5	0x57	-36.0	0x2C	-57.5	0x01	-79.0
0xD7	28.0	0xAC	6.5	0x81	-15.0	0x56	-36.5	0x2B	-58.0	0x00	-295.0
0xD6	27.5	0xAB	6.0	0x80	-15.5	0x55	-37.0	0x2A	-58.5		
0xD5	27.0	0xAA	5.5	0x7F	-16.0	0x54	-37.5	0x29	-59.0		

Table 14. Mixer Gain & Polarity

Index	Polarity	dB	Index	Polarity	dB	Index	Polarity	dB	Index	Polarity	dB
7E	+	18	7D	-	18	3E	+	-4	3D	-	-4
7C	+	17	7B	-	17	3C	+	-4.5	3B	-	-4.5
7A	+	16	79	-	16	3A	+	-5	39	-	-5
78	+	15	77	-	15	38	+	-5.5	37	-	-5.5
76	+	14	75	-	14	36	+	-6	35	-	-6
74	+	13	73	-	13	34	+	-7	33	-	-7
72	+	12	71	-	12	32	+	-8	31	-	-8
70	+	11	6F	-	11	30	+	-9	2F	-	-9
6E	+	10	6D	-	10	2E	+	-10	2D	-	-10
6C	+	9	6B	-	9	2C	+	-11	2B	-	-11
6A	+	8	69	-	8	2A	+	-12	29	-	-12
68	+	7	67	-	7	28	+	-13	27	-	-13
66	+	6	65	-	6	26	+	-14	25	-	-14
64	+	5.5	63	-	5.5	24	+	-15	23	-	-15
62	+	5	61	-	5	22	+	-16	21	-	-16
60	+	4.5	5F	-	4.5	20	+	-17	1F	-	-17
5E	+	4	5D	-	4	1E	+	-18	1D	-	-18
5C	+	3.5	5B	-	3.5	1C	+	-19	1B	-	-19
5A	+	3	59	-	3	1A	+	-20	19	-	-20
58	+	2.5	57	-	2.5	18	+	-21	17	-	-21
56	+	2	55	-	2	16	+	-22	15	-	-22
54	+	1.5	53	-	1.5	14	+	-23	13	-	-23
52	+	1	51	-	1	12	+	-24	11	-	-24
50	+	0.5	4F	-	0.5	10	+	-25	0F	-	-25
4E	+	0	4D	-	0	0E	+	-26	0D	-	-26
4C	+	-0.5	4B	-	-0.5	0C	+	-27	0B	-	-27
4A	+	-1	49	-	-1	0A	+	-28	09	-	-28
48	+	-1.5	47	-	-1.5	08	+	-29	07	-	-29
46	+	-2	45	-	-2	06	+	-30	05	-	-30
44	+	-2.5	43	-	-2.5	04	+	-31	03	-	-31
42	+	-3	41	-	-3	02	+	-32	01	-	-32
40	+	-3.5	3F	-	-3.5	00	+	-150			

Table 15. Auto Mute Detection Threshold Table

Name	Description	Value	dB
AT	Auto-mute Detection threshold	0000	-126
		0001	-120
		0010	-114
		0011	-108
		0100	-102
		0101	-96
		0110	-90
		0111	-84
		1000	-78
		1001	-72
		1010	-66
		1011	-60
		1100	-54
		1101	-48
		1110	-42
		1111	**Auto-mute**

※ **Do not use value 1111.**

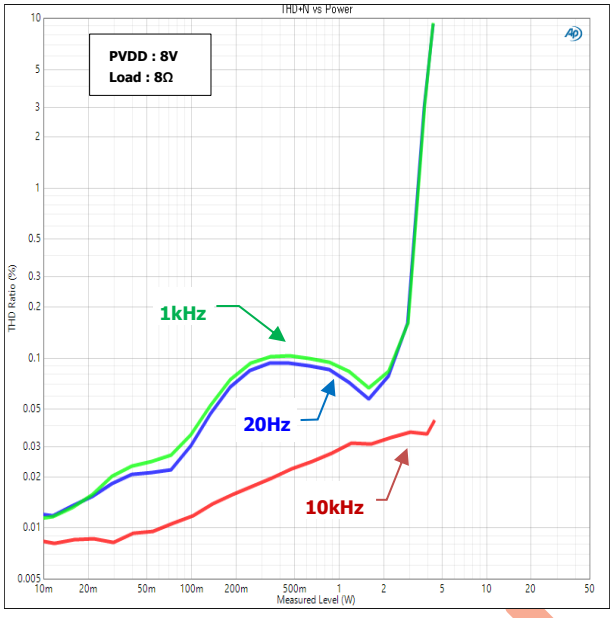
Table 16. Power Meter Reading Table

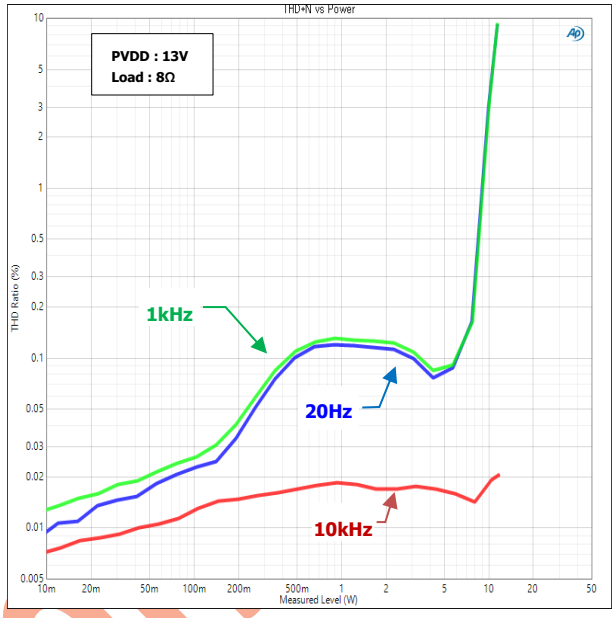
addr 0x2F (Decimal)	addr 0x2F (Hex)	dB	addr 0x2F (Decimal)	addr 0x2F (Hex)	dB	addr 0x2F (Decimal)	addr 0x2F (Hex)	dB	addr 0x2F (Decimal)	addr 0x2F (Hex)	dB
0	0x00	-0.0	64	0x40	-32.0	128	0x80	-64.0	192	0xC0	-96.0
1	0x01	-0.5	65	0x41	-32.5	129	0x81	-64.5	193	0xC1	-96.5
2	0x02	-1.0	66	0x42	-33.0	130	0x82	-65.0	194	0xC2	-97.0
3	0x03	-1.5	67	0x43	-33.5	131	0x83	-65.5	195	0xC3	-97.5
4	0x04	-2.0	68	0x44	-34.0	132	0x84	-66.0	196	0xC4	-98.0
5	0x05	-2.5	69	0x45	-34.5	133	0x85	-66.5	197	0xC5	-98.5
6	0x06	-3.0	70	0x46	-35.0	134	0x86	-67.0	198	0xC6	-99.0
7	0x07	-3.5	71	0x47	-35.5	135	0x87	-67.5	199	0xC7	-99.5
8	0x08	-4.0	72	0x48	-36.0	136	0x88	-68.0	200	0xC8	-100.0
9	0x09	-4.5	73	0x49	-36.5	137	0x89	-68.5	201	0xC9	-100.5
10	0x0A	-5.0	74	0x4A	-37.0	138	0x8A	-69.0	202	0xCA	-101.0
11	0x0B	-5.5	75	0x4B	-37.5	139	0x8B	-69.5	203	0xCB	-101.5
12	0x0C	-6.0	76	0x4C	-38.0	140	0x8C	-70.0	204	0xCC	-102.0
13	0x0D	-6.5	77	0x4D	-38.5	141	0x8D	-70.5	205	0xCD	-102.5
14	0x0E	-7.0	78	0x4E	-39.0	142	0x8E	-71.0	206	0xCE	-103.0
15	0x0F	-7.5	79	0x4F	-39.5	143	0x8F	-71.5	207	0xCF	-103.5
16	0x10	-8.0	80	0x50	-40.0	144	0x90	-72.0	208	0xD0	-104.0
17	0x11	-8.5	81	0x51	-40.5	145	0x91	-72.5	209	0xD1	-104.5
18	0x12	-9.0	82	0x52	-41.0	146	0x92	-73.0	210	0xD2	-105.0
19	0x13	-9.5	83	0x53	-41.5	147	0x93	-73.5	211	0xD3	-105.5
20	0x14	-10.0	84	0x54	-42.0	148	0x94	-74.0	212	0xD4	-106.0
21	0x15	-10.5	85	0x55	-42.5	149	0x95	-74.5	213	0xD5	-106.5
22	0x16	-11.0	86	0x56	-43.0	150	0x96	-75.0	214	0xD6	-107.0
23	0x17	-11.5	87	0x57	-43.5	151	0x97	-75.5	215	0xD7	-107.5
24	0x18	-12.0	88	0x58	-44.0	152	0x98	-76.0	216	0xD8	-108.0
25	0x19	-12.5	89	0x59	-44.5	153	0x99	-76.5	217	0xD9	-108.5
26	0x1A	-13.0	90	0x5A	-45.0	154	0x9A	-77.0	218	0xDA	-109.0
27	0x1B	-13.5	91	0x5B	-45.5	155	0x9B	-77.5	219	0xDB	-109.5
28	0x1C	-14.0	92	0x5C	-46.0	156	0x9C	-78.0	220	0xDC	-110.0
29	0x1D	-14.5	93	0x5D	-46.5	157	0x9D	-78.5	221	0xDD	-110.5
30	0x1E	-15.0	94	0x5E	-47.0	158	0x9E	-79.0	222	0xDE	-111.0
31	0x1F	-15.5	95	0x5F	-47.5	159	0x9F	-79.5	223	0xDF	-111.5
32	0x20	-16.0	96	0x60	-48.0	160	0xA0	-80.0	224	0xE0	-112.0
33	0x21	-16.5	97	0x61	-48.5	161	0xA1	-80.5	225	0xE1	-112.5
34	0x22	-17.0	98	0x62	-49.0	162	0xA2	-81.0	226	0xE2	-113.0
35	0x23	-17.5	99	0x63	-49.5	163	0xA3	-81.5	227	0xE3	-113.5
36	0x24	-18.0	100	0x64	-50.0	164	0xA4	-82.0	228	0xE4	-114.0
37	0x25	-18.5	101	0x65	-50.5	165	0xA5	-82.5	229	0xE5	-114.5
38	0x26	-19.0	102	0x66	-51.0	166	0xA6	-83.0	230	0xE6	-115.0
39	0x27	-19.5	103	0x67	-51.5	167	0xA7	-83.5	231	0xE7	-115.5
40	0x28	-20.0	104	0x68	-52.0	168	0xA8	-84.0	232	0xE8	-116.0
41	0x29	-20.5	105	0x69	-52.5	169	0xA9	-84.5	233	0xE9	-116.5
42	0x2A	-21.0	106	0x6A	-53.0	170	0xAA	-85.0	234	0xEA	-117.0
43	0x2B	-21.5	107	0x6B	-53.5	171	0xAB	-85.5	235	0xEB	-117.5
44	0x2C	-22.0	108	0x6C	-54.0	172	0xAC	-86.0	236	0xEC	-118.0
45	0x2D	-22.5	109	0x6D	-54.5	173	0xAD	-86.5	237	0xED	-118.5
46	0x2E	-23.0	110	0x6E	-55.0	174	0xAE	-87.0	238	0xEE	-119.0
47	0x2F	-23.5	111	0x6F	-55.5	175	0xAF	-87.5	239	0xEF	-119.5
48	0x30	-24.0	112	0x70	-56.0	176	0xB0	-88.0	240	0xF0	-120.0
49	0x31	-24.5	113	0x71	-56.5	177	0xB1	-88.5	241	0xF1	-120.5
50	0x32	-25.0	114	0x72	-57.0	178	0xB2	-89.0	242	0xF2	-121.0
51	0x33	-25.5	115	0x73	-57.5	179	0xB3	-89.5	243	0xF3	-121.5
52	0x34	-26.0	116	0x74	-58.0	180	0xB4	-90.0	244	0xF4	-122.0
53	0x35	-26.5	117	0x75	-58.5	181	0xB5	-90.5	245	0xF5	-122.5
54	0x36	-27.0	118	0x76	-59.0	182	0xB6	-91.0	246	0xF6	-123.0
55	0x37	-27.5	119	0x77	-59.5	183	0xB7	-91.5	247	0xF7	-123.5
56	0x38	-28.0	120	0x78	-60.0	184	0xB8	-92.0	248	0xF8	-124.0
57	0x39	-28.5	121	0x79	-60.5	185	0xB9	-92.5	249	0xF9	-124.5
58	0x3A	-29.0	122	0x7A	-61.0	186	0xBA	-93.0	250	0xFA	-125.0
59	0x3B	-29.5	123	0x7B	-61.5	187	0xBB	-93.5	251	0xFB	-125.5
60	0x3C	-30.0	124	0x7C	-62.0	188	0xBC	-94.0	252	0xFC	-126.0
61	0x3D	-30.5	125	0x7D	-62.5	189	0xBD	-94.5	253	0xFD	-126.5
62	0x3E	-31.0	126	0x7E	-63.0	190	0xBE	-95.0	254	0xFE	-127.0
63	0x3F	-31.5	127	0x7F	-63.5	191	0xBF	-95.5	255	0xFF	< -127.5

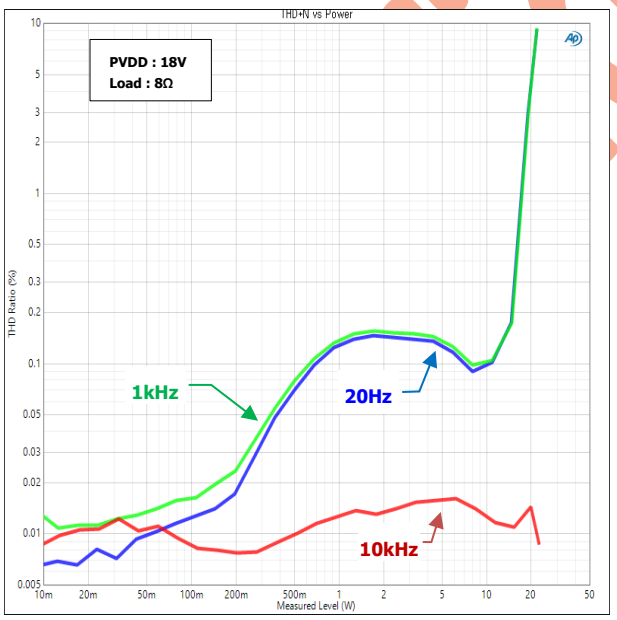
※ Output 8bit value : (-dB * 2), n dB = output 8bit *0.5

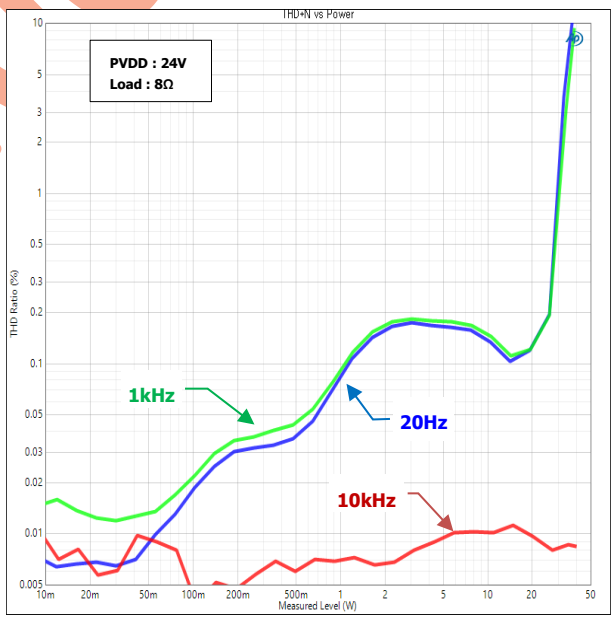
C. Typical Characteristics Graph

Total Harmonic Distortion + Noise vs. Power, BTL D-BTL Mode Configuration, 8Ω

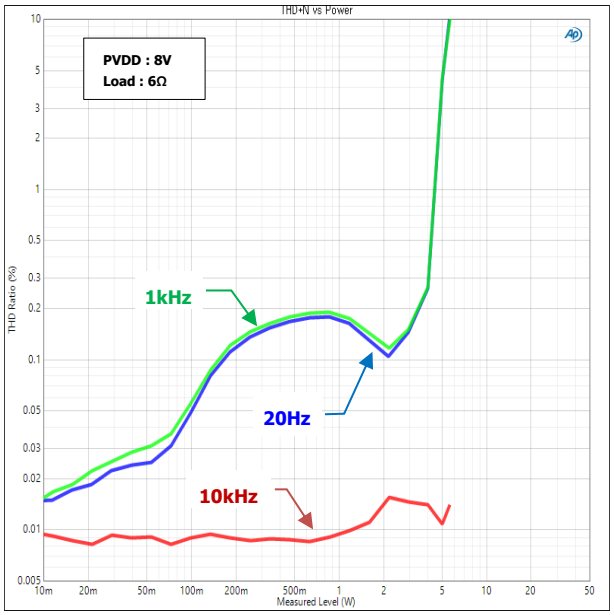


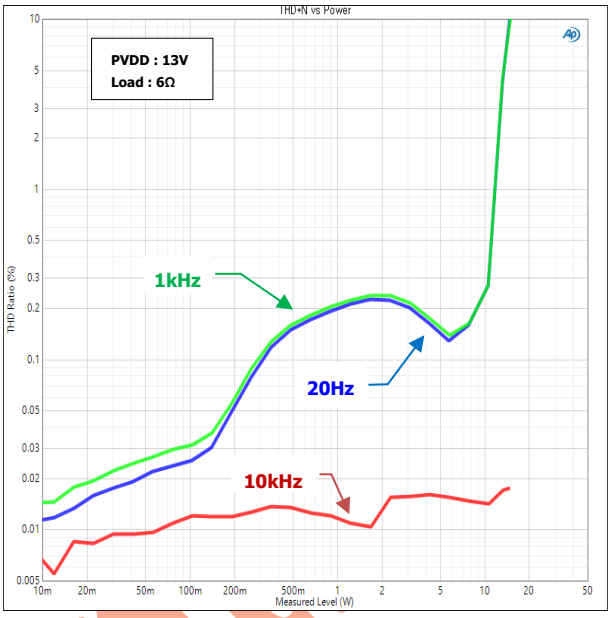


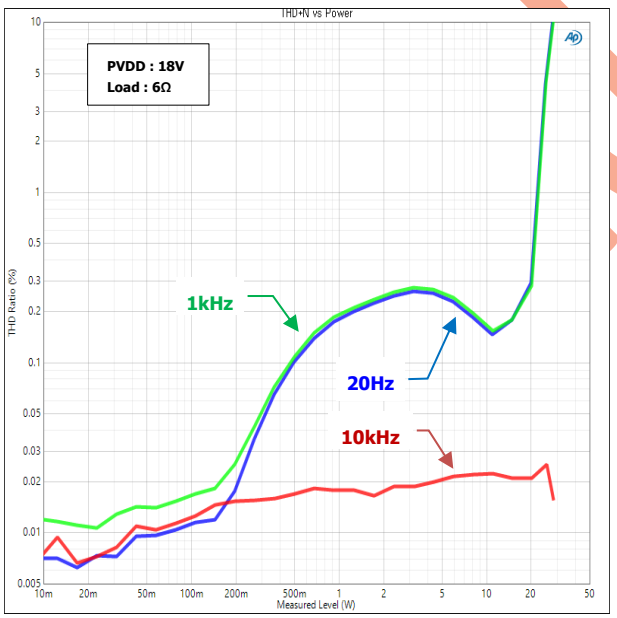


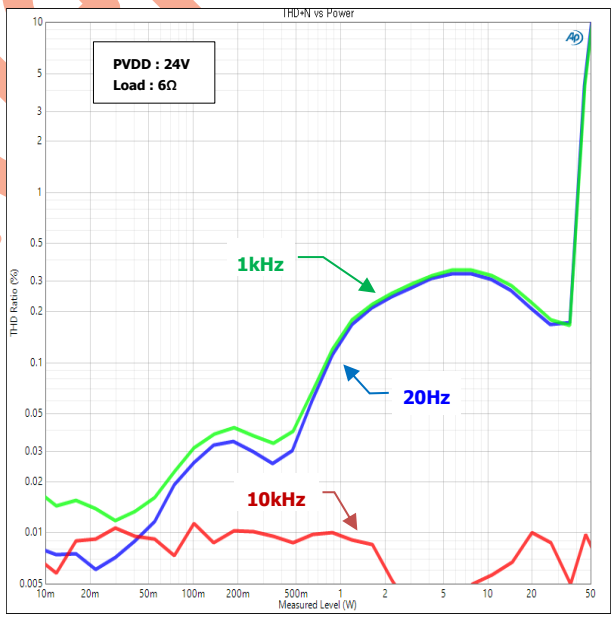


Total Harmonic Distortion + Noise vs. Power, BTL D-BTL Mode Configuration, 6Ω

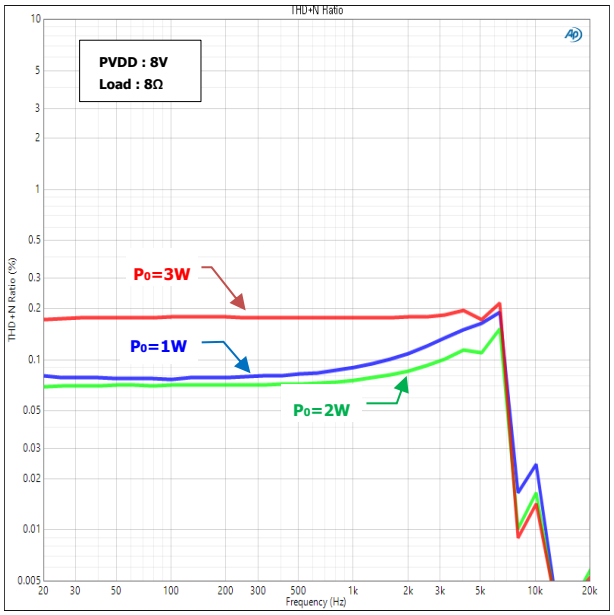


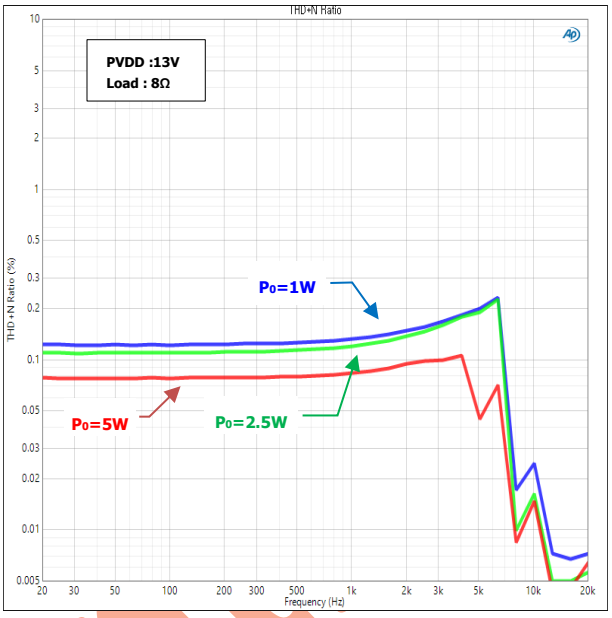


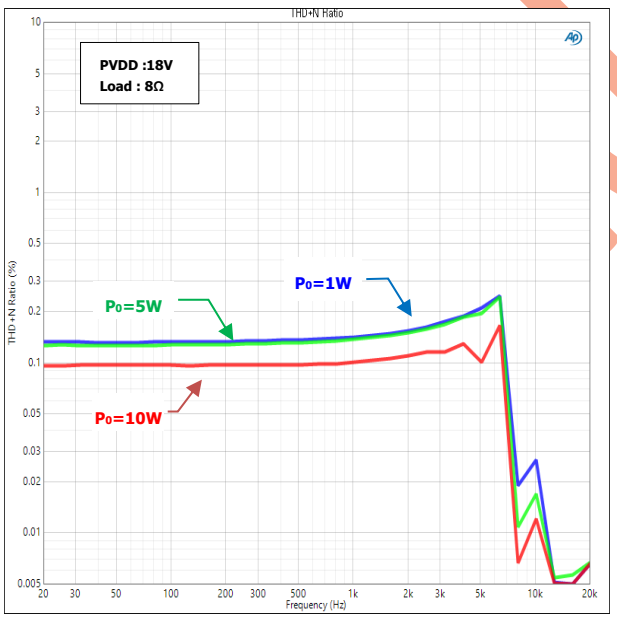


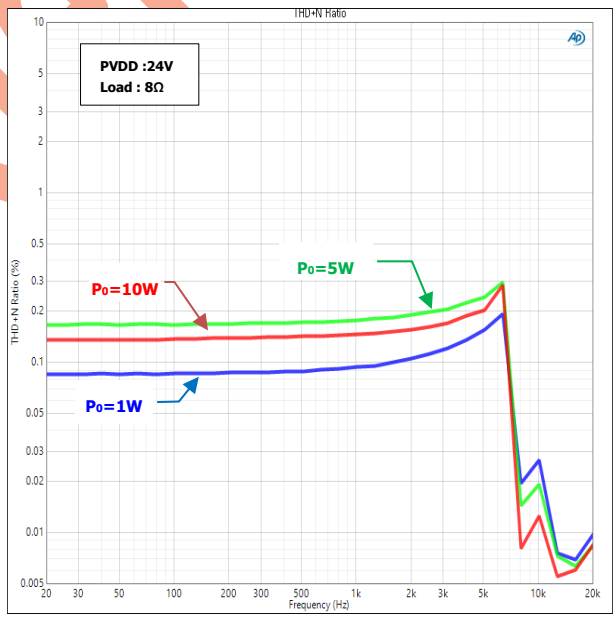


Total Harmonic Distortion + Noise vs. Frequency, BTL D-BTL Mode Configuration, 8Ω

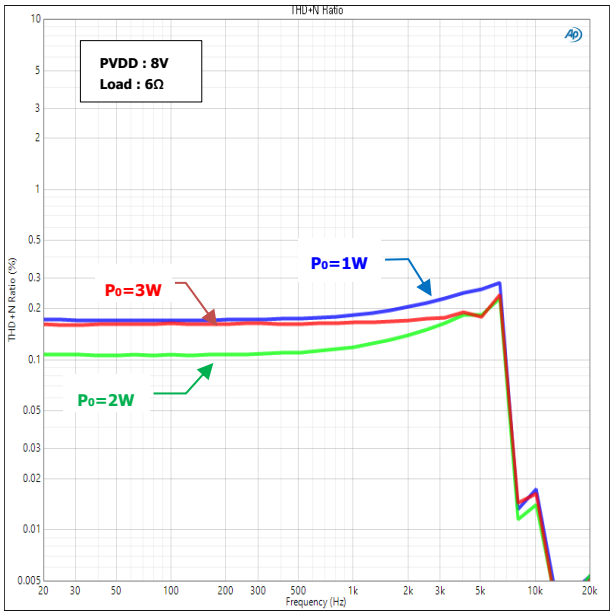


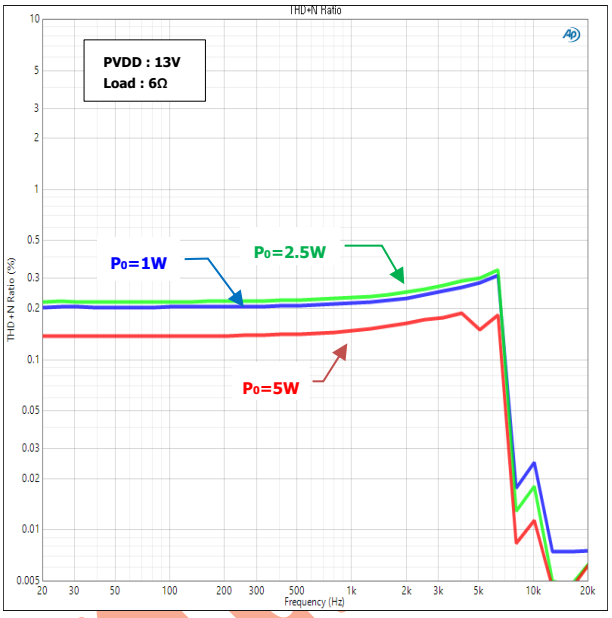


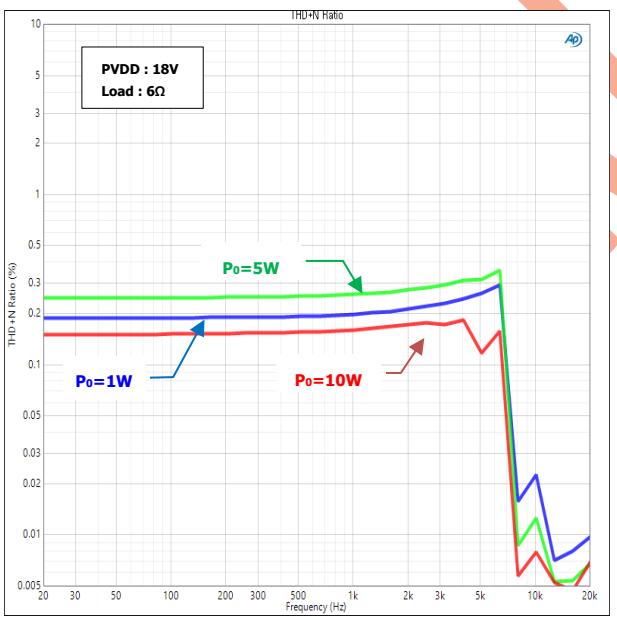


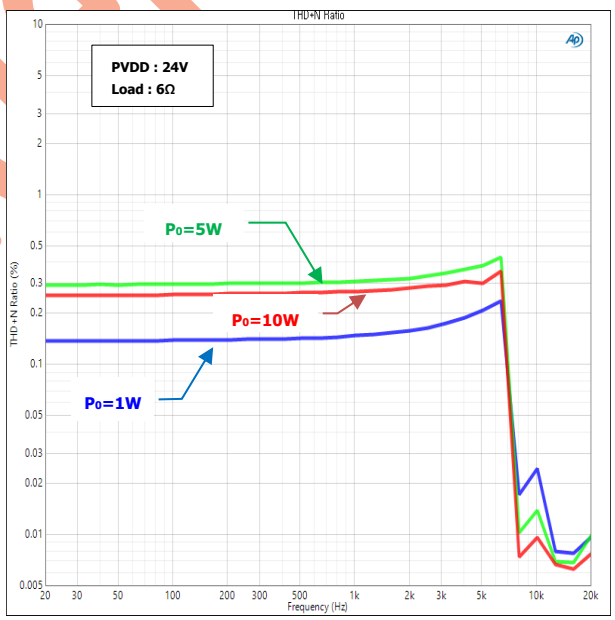


Total Harmonic Distortion + Noise vs. Frequency, BTL D-BTL Mode Configuration, 6Ω

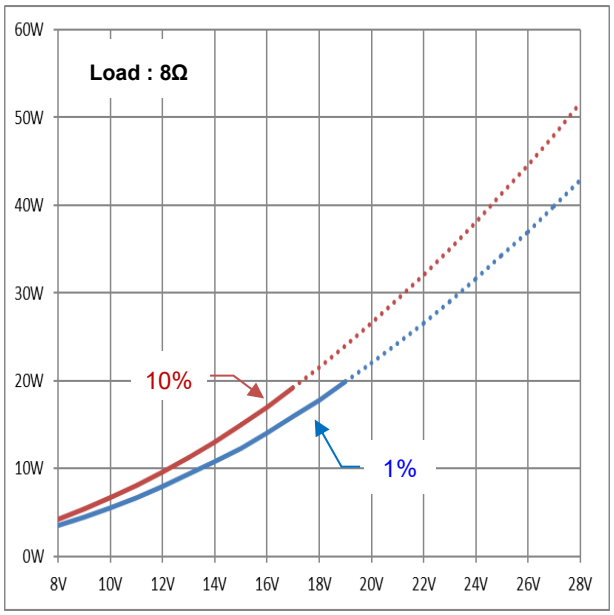


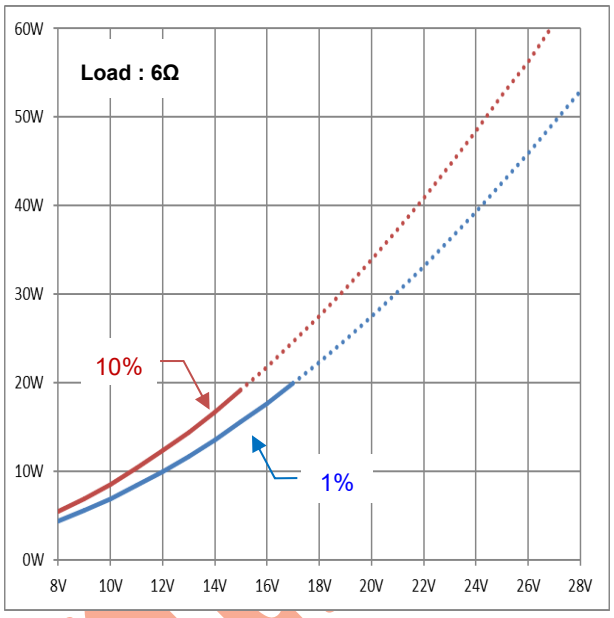




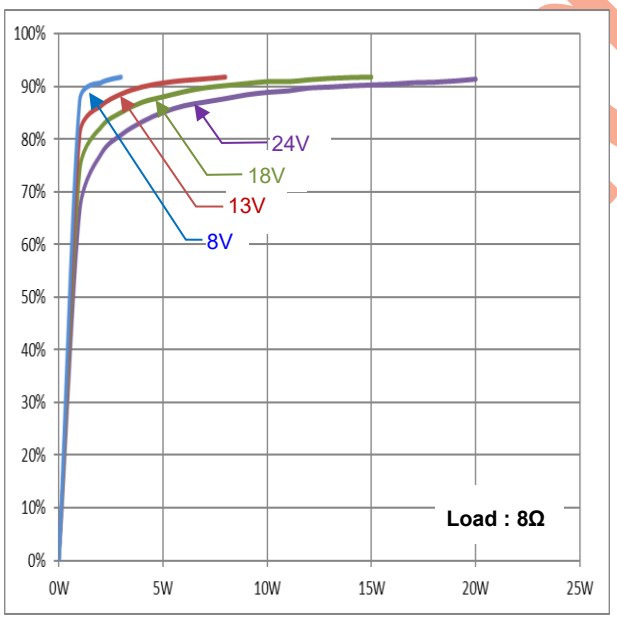


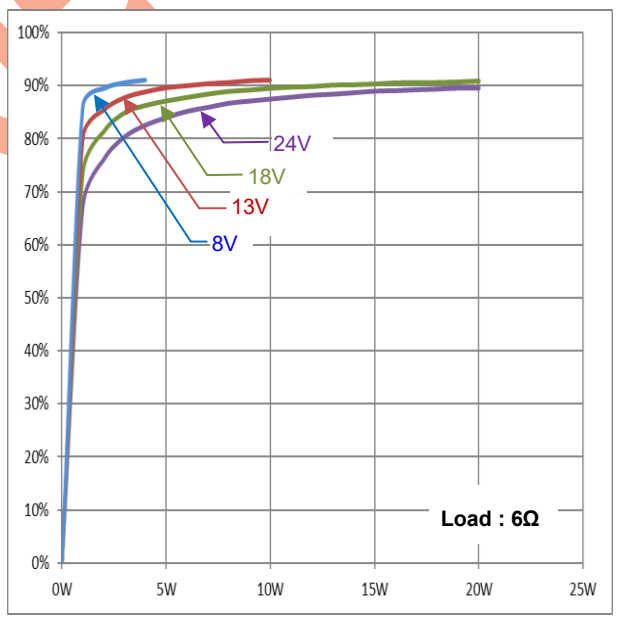
Output Power vs. PVDD, BTL D-BTL Mode Configuration



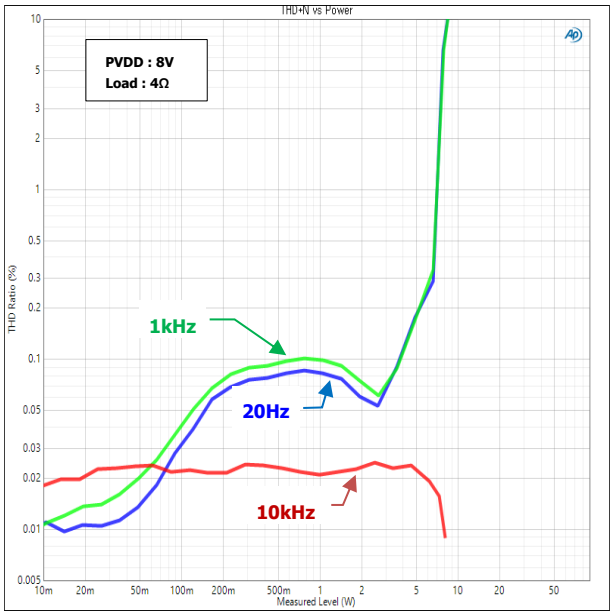


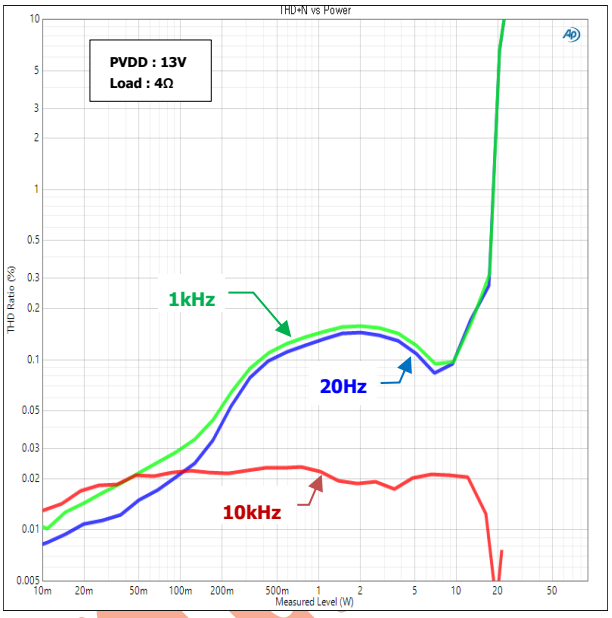
Efficiency vs. Total Power, BTL D-BTL Mode Configuration

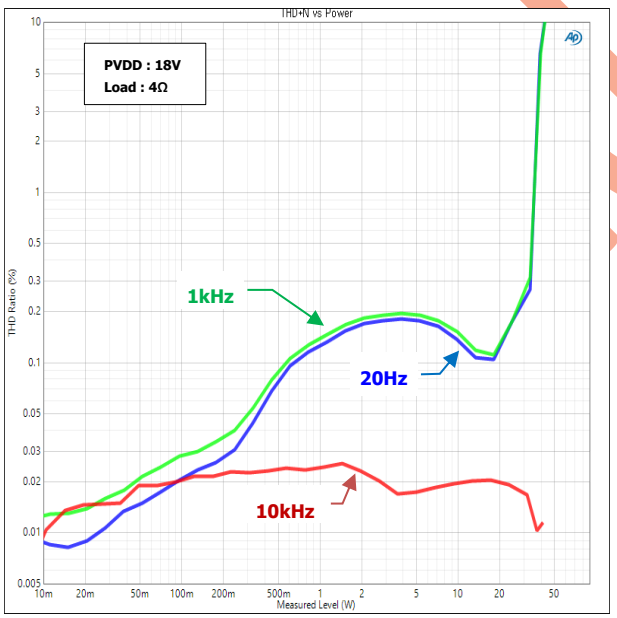


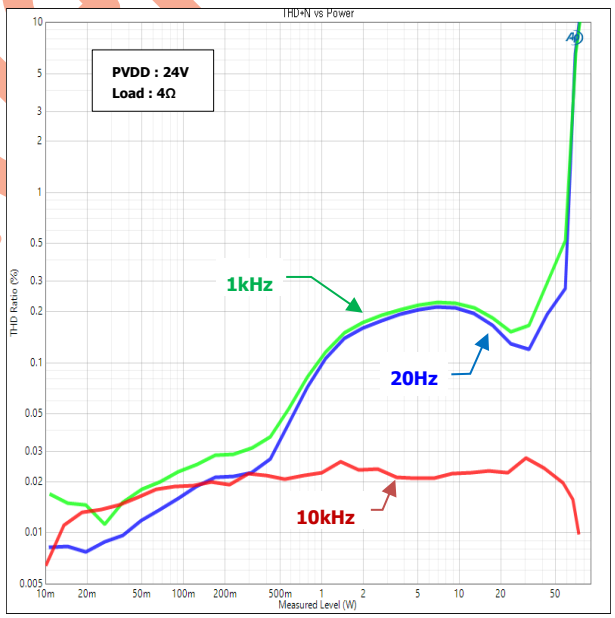


Total Harmonic Distortion + Noise vs. Power, PBTL D-BTL Mode Configuration, 4Ω

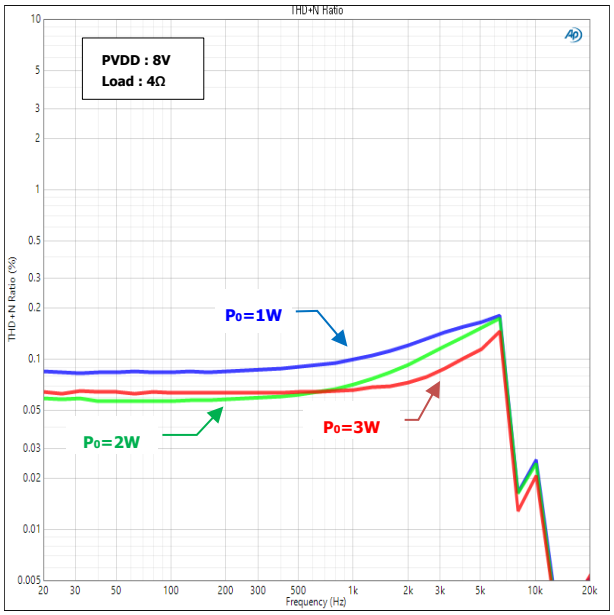


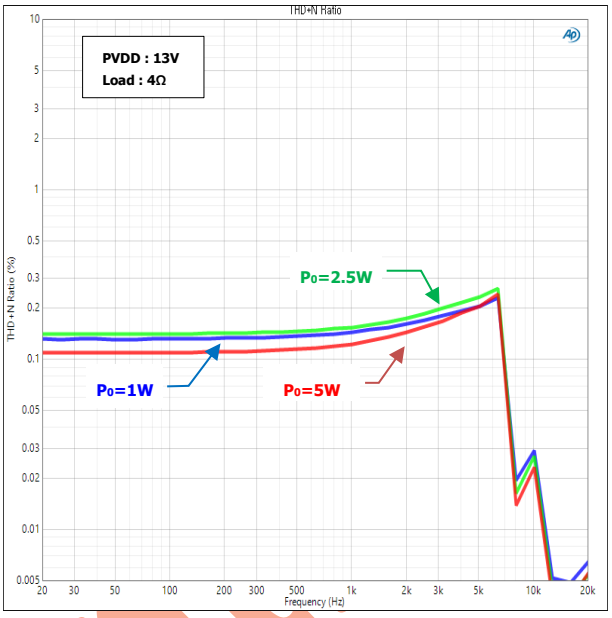


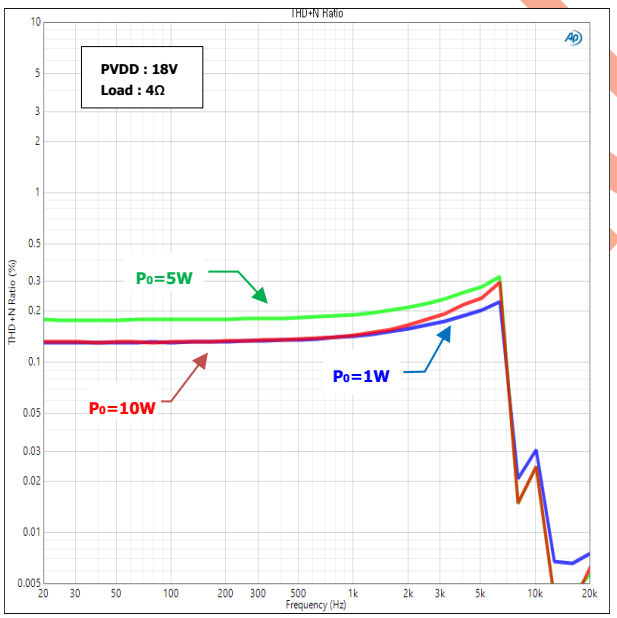


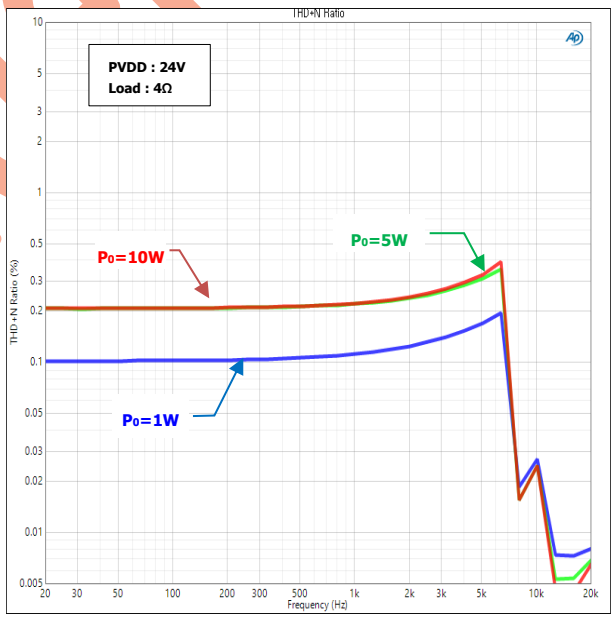


Total Harmonic Distortion + Noise vs. Frequency, PBTL D-BTL Mode Configuration, 4Ω

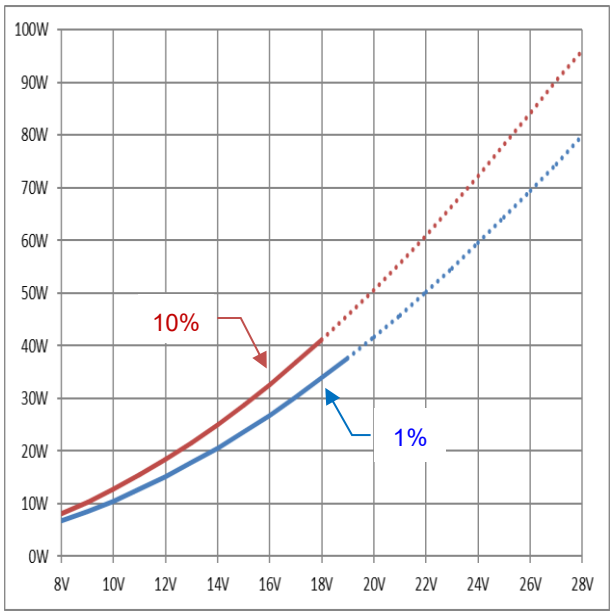








Output Power vs. PVDD, PBTL D-BTL Mode Configuration



Efficiency vs. Total Power, PBTL D-BTL Mode Configuration