Product information presented is for internal use within CHIPONE only. Details are subject to change without notice

19-CH LEVEL SHIFTER FOR GOA TFT-LCD PANEL

FEATURES

- **2.6V to 5.5V Input Logic Level Range**
- **-20V to 45V Output Voltage Range**
- **19 Ch Level Shifter Support 12-CH CLK, 3-CH LS_STV, VDDE/VDDO, LS_VGL, LS_LVGL**
- **Protection Functions: UVLO, OTP, OCP**
- **Support 2 IN, 4/6/8/10/12 CLK OUT**
- **CLK Charge Sharing & GPM Function**
- **I2C Interface**
- **Power Off Discharge Option**
- **RoHS Compliant and Halogen Free**

GENERAL DESCRIPTION

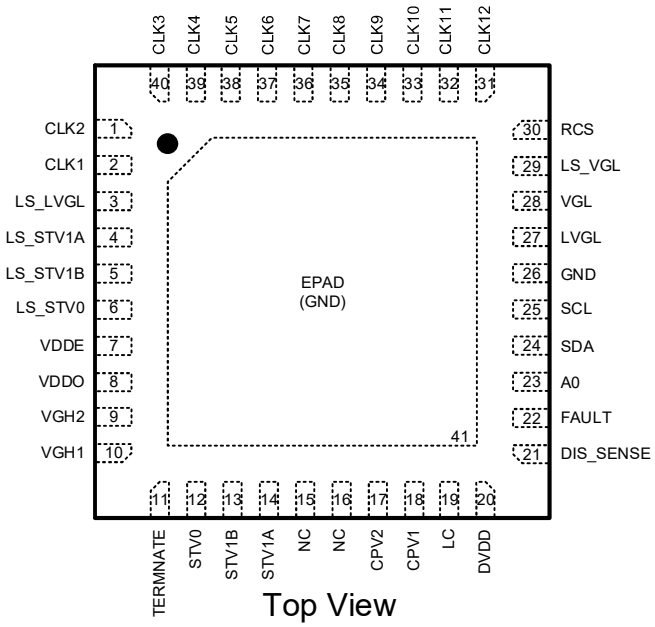
The iML7276 is a 19 channel high-voltage level-shifter application. The device converts logic level signals generated by the Timing Controller (TCON) to high level signals used by the display panel. With being available in a WQFN-40L 5x5 package, this device is suitable for GOP TFT-LCD panel.

Level shifter is designed for generating a high voltage signal to drive the TFT-LCD panel. The iML7276 includes 8 GOA input signal (CPV1 to CPV2, STV0, STV1A, STV1B, LC, TERMINATE, DIS_SENSE), 19- CH GOA output signal (12CLK, LS_STV0, LS_STV1A, LS_STV1B, VDDE, VDDO, LS_VGL and LS_LVGL. It also integrates reset function. As long as DVDD reaches discharge level, all channels will be pulled to VGH.

APPLICATIONS

GOA TFT-LCD Panel

PIN CONFIGURATION



Top View

ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
iML7276	iML7276GD-TR	QFNWB5x5_40L	Tape and Reel	–40 °C to +85 °C	i7276 ZYYWWXXX	i7276: Part Name YYWW: Date code ZXXX: Tracking Number.

Note: All CHIPONE products are lead free and halogen free.

TYPICAL APPLICATION

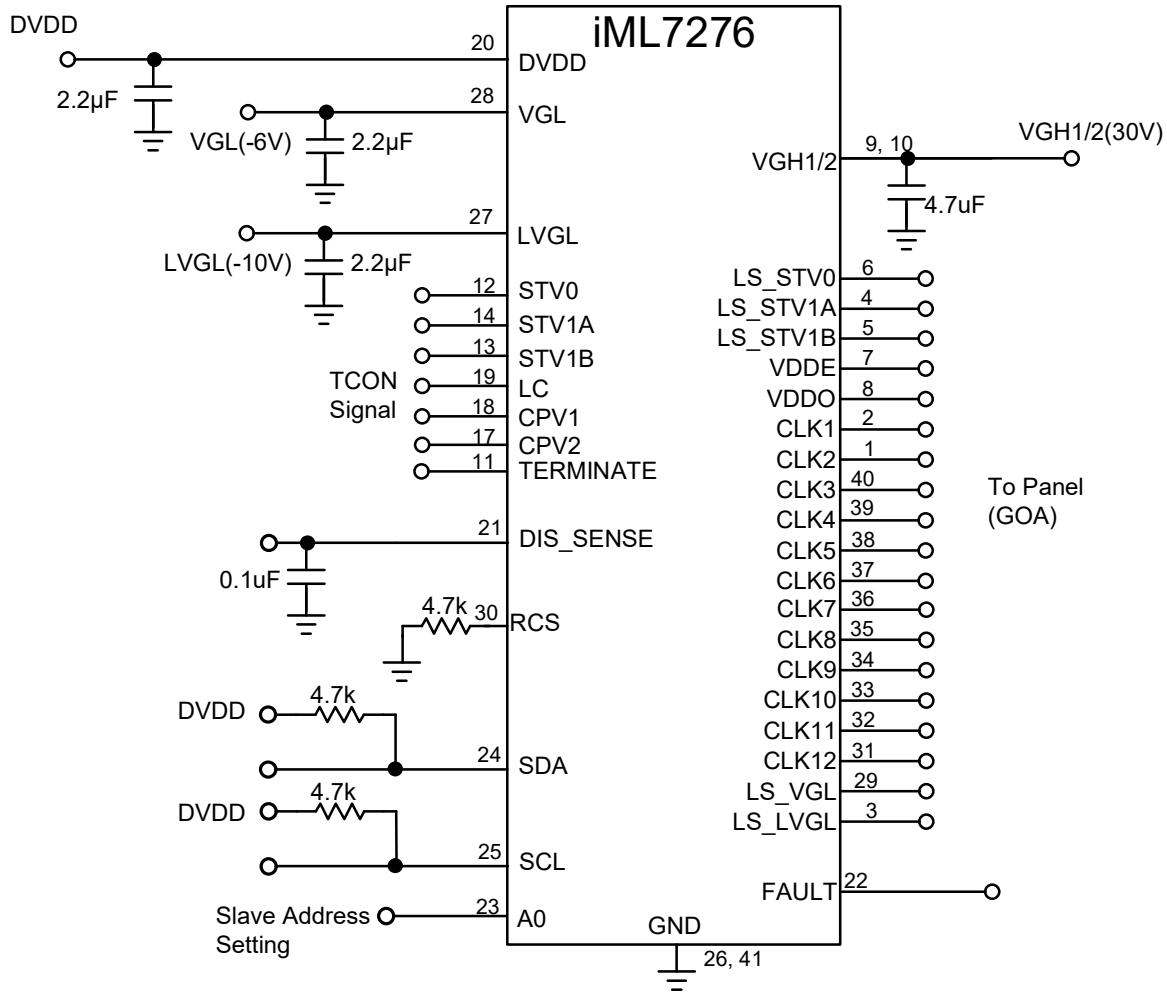


Figure 1 The iML7276 Application Circuit

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Input Voltage: VDD, SDA, SCL (continuous)	V_{IN}	–0.3 to +7	V
Ground Voltage	V_{GND}	–0.3 to +0.3	V
STV0, STV1A, STV1B, LC, CPV1, and CPV2 to GND	V_{L1}	–0.3 to +7	V
DIS_SENSE, A0, FAULT, TERMINATE to GND	V_{L2}	–0.3 to +7	V
VGH1/2 to GND	V_{H1}	–0.3 to +45	V
VGL, LVGL to GND	V_{H2}	–22 to +0.3	V
(VGH1 or VGH2) – (VGL or LVGL)	V_{H3}	–0.3 to +65	V
LS_STV1A, LS_STV1B to GND	V_{H4}	(LVGL + 0.3V) to (VGH1 - 0.3V)	V
CLK1~CLK12, LS_LVGL to GND	V_{H5}	(LVGL + 0.3V) to (VGH1 - 0.3V)	V
VDDE, VDDO, LS_STV0 to GND	V_{H6}	(LVGL + 0.3V) to (VGH2 - 0.3V)	V
LS_VGL to GND	V_{H7}	(VGL + 0.3V) to (VGH1 - 0.3V)	V
Power Dissipation, @ T_A = +25°C , T_J = +125°C	P_d	3.63	W
Package Thermal Resistance (Note 2)	θ_{JA}	27.5	°C /W
Package Thermal Resistance (Note 2)	θ_{JC}	6	°C /W
Lead Temperature (Soldering, 10sec..)		260	°C
Junction Temperature		150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
ESD Machine Model	MM	400	V
ESD Susceptibility Human Body Model (Note 3) (LS_STV0/1A/1B, VDDE/VDDO, LS_LVGL/LS_VGL, CLK1 to CLK12 to GND)	HBM	8k	V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Ambient Temperature Range (Note 4)		–40 to +85	°C
Junction Temperature Range (Note 4)		–40 to +125	°C

Notes:

1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2. θJA is measured under natural convection (still air) at TA= 25°C with the component mounted on a high effective thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θJC is measured at the exposed pad of the package.

3. Devices are ESD sensitive. Handing precaution is recommended.

4. The device is not guaranteed to function outside its operating conditions.

ELECTRICAL CHARACTERISTICS

DVDD=3.3V, VGH=30V, LVGL=-10V, VGL=-6V, GND=0V, TA=+25°C unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Supply Current						
Supply Voltage	VDD		2.6	--	5.5	V
VDD Quiescent Current	IQ-VDD	DIS_SENSE=High	--	4.2	--	mA
VGH1 Quiescent Current	IQ-VGH1	DIS_SENSE=High	--	0.25	--	mA
VGH2 Quiescent Current	IQ-VGH2	DIS_SENSE=High	--	0.25	--	mA
VGL Quiescent Current	IQ-VGL	DIS_SENSE=High	--	25	--	uA
LVGL Quiescent Current	IQ-LVGL	DIS_SENSE=High	--	0.5	--	mA
Protections						
DVDD Under-Voltage Lockout Threshold	$V_{UVLO-VDD}$	VDD rising, Hysteresis 200mV	1.7	2.0	2.3	V
		VDD falling	1.5	1.8	2.1	V
VGH1 Under-Voltage Lockout Threshold	V_{UVLOGH}	VGH1 rising, 03h[2]=1	14	15	16	V
		VGH1 rising, 03h[2]=0	7	8	9	V
		VGH1 falling	4	5	6	
POR Under-Voltage Lockout Threshold	$V_{UVLOPOR}$	POR falling	--	3.5	--	V
Thermal Shutdown	T_{SD}	Junction temperature rising	150	--	180	°C
Thermal Shutdown Hysteresis	HYTSD		--	20	--	°C
Internal Pull-Down Resistor (CPV1 to CPV2, LC, STV0/1A/1B, TERMINATE)			--	400	--	kΩ
A0, FAULT Internal Pull Up Resistor			--	200	--	kΩ
Level Shifter						
VGH1/2 to GND	VGH		10	--	45	V
VGL Operating Voltage Range	VGL	(Note 5)	-20	--	0	V
LVGL Operating Voltage Range	LVGL	(Note 5)	-20	--	0	V
VGH1/2-LVGL/VGL	V_{HL}		--	--	60	V
CPV1 to CPV2, TERMINATE, ST0, STV1A, STV1B, LC, A0	VIH	VDD = 2.3V to 5.5V	1.2	--	--	V
	VIL	VDD = 2.3V to 5.5V	--	--	0.8	V
DIS_SENSE Threshold Voltage	$V_{DIS\_SENSE\_R}$	DIS_SENSE rising	--	1	--	V

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
	$V_{DIS\_SENSE\_F}$	DIS_SENSE falling	--	0.8	--	
CPV1 to CPV2, TERMINATE, ST0, STV1A, STV1B, LC, A0 Input Signal Pulse width Signal Pulse Width (Note 6)	VIW	VDD = 2.3V to 5.5V	200	--	--	ns
CPV1 to CPV2 Input signal Maximum Frequency	Fc		--	--	800	kHz
CLK1 to CLK12, LS_STV0/1A/1B, Positive Output Swing	VCK1+	All inputs high, IO = 10mA	VGH1 -0.2	VGH1 -0.15	VGH1	V
VDDE, VDDO and LS_STV0 Positive Output Swing	VCK2+	All inputs high, IO = 10mA	VGH2 -0.2	VGH2 -0.15	VGH2	V
CLK1 to CLK12, LS_STV0, LS_STV1A, LS_STV1B, VDDE, and VDDO Negative Output Swing	VCK-	All inputs low, IO = -10mA	LVGL +0.2	LVGL +0.15	LVGL	V
LS_VGL, LS_LVGL High-Side Ron	RON_{HS}		--	25	--	Ω
LS_VGL, LS_LVGL Low-Side Ron	RON_{LS}		--	10	25	Ω
CLK1 to CLK12, LS_STV0, LS_STV1A, LS_STV1B, VDDE, VDDO, LS_VGL, LS_LVGL, OCP Level	OCP	02h[2:0] and 02h[5:3]=000	Disable OCP			-
		02h[2:0] and 02h[5:3]=001	10	20	30	mA
		02h[2:0] and 02h[5:3]=010	20	30	40	mA
		02h[2:0] and 02h[5:3]=011	40	50	60	mA
		02h[2:0] and 02h[5:3]=100	60	70	80	mA
		02h[2:0] and 02h[5:3]=101	77	90	103	mA
		02h[2:0] and 02h[5:3]=110	102	120	138	mA
		02h[2:0] and 02h[5:3]=111	136	160	184	mA
CLK1 to CLK12 Rising Slew Rate (Note 7) (Note 8)	t_{R1}	VGH = 30V, LVGL = -10V, VGL=-6V, RL = 51ohm, CL = 4.7nF, 20% to 80%	--	1500	--	V/us
	t_{R2}	VGH = 30V, LVGL = -10V, VGL=-6V, RL = 51ohm, CL = 4.7nF, 20% to 80%	--	1000	--	V/us
	t_{R3}	VGH = 30V, LVGL = -10V, VGL=-6V, RL = 51ohm, CL = 4.7nF, 20% to 80%	--	500	--	V/us
	t_{R4}	VGH = 30V, LVGL = -10V, VGL=-6V, RL = 51ohm, CL = 4.7nF, 20% to 80%	--	100	--	V/us
CLK1 to CLK12 Falling Slew Rate (Note 7) (Note 8)	t_{F1}	VGH = 30V, LVGL = -10V, VGL=-6V, RL = 51ohm, CL = 4.7nF, 80% to 20%	--	1500	--	V/us
	t_{F2}	VGH = 30V, LVGL = -10V, VGL=-6V, RL = 51ohm, CL = 4.7nF, 80% to 20%	--	1000	--	V/us
	t_{F3}	VGH = 30V, LVGL = -10V, VGL=-6V, RL = 51ohm, CL = 4.7nF, 80% to 20%	--	500	--	V/us

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
	t_{F4}	VGH = 30V, LVGL = -10V, VGL=-6V, RL = 51ohm, CL = 4.7nF, 80% to 20%	--	100	--	V/us
LS_STV0, LS_STV1A, LS_STV1B, VDDE, VDDO, Rising / Falling Slew Rate (Note 8)	tR	VGH = 30V, LVGL = -10V, VGL=-6V, RL = 51ohm, CL = 4.7nF, 20% to 80%	--	300	--	V/us
	tF	VGH = 30V, LVGL = -10V, VGL=-6V, RL = 51ohm, CL = 4.7nF, 80% to 20%	--	300	--	V/us
CLK1 to CLK12, LS_STV0, LS_STV1A, LS_STV1B, VDDE, and VDDO Rising / Falling Edge Delay Time	tRD	DVDD=5V, VGH = 30V, LVGL = -10V, VGL=-6V, 50% of input to 10% of output	--	80	100	ns
	tFD	DVDD=5V, VGH = 30V, LVGL = -10V, VGL=-6V, 50% of input to 90% of output	--	80	100	ns
CLK High Side Detection Time(Note10)	CLK_{hde}	Error=±40% for 0.5us/1us Error=±20% for other	0.5	--	8	us
CLK Low Side Detection Time	CLK_{lde}	Error=±40% for 0.5us/1us Error=±20% for other	0.5	--	8	us
LS_STV0, LS_STV1A, LS_STV1B High Side Detection Time(Note10)	LS_STV0/STV1A/STV1B hde	Error=±40% for 0.5us/1us Error=±20% for other	0.5	--	8	us
LS_STV0, LS_STV1A, LS_STV1B Low Side Detection Time	LS_STV0/STV1A/STV1B lde		--	40	--	us
VDDE/VDDO High Side Detect Time	VDDE/VDDO hde		--	40	--	us
VDDE/VDDO Low Side Detect Time	VDDE/VDDO lde		--	40	--	us
LS_VGL, LS_LVGL Low Side Detect Time	LS_VGL/LS_LVGL lde		--	40	--	us
Input Threshold (SCL, SDA, EN)						
Input Low Voltage	VIL		-	-	0.8	V
Input High Voltage	VIH		1.5	-	-	V
I²C Interface						
SCL, SDA Input Capacitance	C_{SI}		-	5	-	pF
SDA Output Low Voltage	V_{OL}	I_{SINK} = 3mA	0	-	0.4	V
SDA, SCL Input Leakage Current	ILK	SCL=SDA=VL or GND	-1	-	1	μA
SCL Clock Frequency	f_{OSCI2C}		1	-	400k	Hz
SCL Clock High Period	t_{IH3}		0.6	-	-	μs
SCL Clock Low Period	t_{IL3}		1.3	-	-	μs
SCL, SDA Receiving Rise Time	t_{R1}		-	20+0.1* C_B	300	ns

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCL, SDA Receiving Fall Time	t_{F1}		-	20+0.1* C_B	300	ns
I²C Data Setup Time	t_{S1}		100	-	-	ns
I²C Data Hold Time	t_{H1}		0	-	900	ns
I²C Setup Time for START Condition	t_{S2}		0.6	-	-	μs
I²C Hold Time for START Condition	t_{H2}		0.6	-	-	μs
STOP Condition Setup Time	t_{SU_STO}		0.6			μs
I²C Bus Free Time Between STOP and START Conditions	t_{BUS}		1.3	-	-	μs
I²C Pulse Width of Suppressed Spike	t_{PS}		-	85	-	ns
I2C Deglitch Time	t_{DEG}		-	50	-	ns
Power On Re-load Time	Tload		-	0.75	1.5	ms
I²C Bus Capacitance	C_B		-	-	400	pF

Notes

5.The sequence of LVGL must be earlier than (or equal to) VGL in application. The voltage of LVGL must be lower than (or equal to) VGL always. If LVGL-VGL>0.3V, abnormal IC function behavior maybe happen.
6.The input signal pulse width must be over 200ns.
7. Rising/Falling time measure point is before RC.
8. STV, CPV, LC delay time of inputsignal to output signal ≤100ns
9. CLK1 to CLK12 Slew Rate can select by 00h[3:2].
10. CLK High/Low-Side and STV0/1A/1B High-Side detect time can select by 02h[2:0].

PIN DESCRIPTION

PIN #	NAME	I/O	DESCRIPTION
1	CLK2	O	Level shifter output.
2	CLK1	O	Level shifter output.
3	LS_LVGL	O	Discharge function for liquid crystal capacitor.
4	LS_STV1A	O	Level shifter output signal. (Start pulse for GOA)
5	LS_STV1B	O	Level shifter output signal. (Start pulse for GOA)
6	LS_STV0	O	Level shifter output signal. (GOA reset signal)
7	VDDE	O	Level shifter output signal. (Low frequency VDDE)
8	VDDO	O	Level shifter output signal. (Low frequency VDDO)
9	VGH2	P	VDDE/VDDO, and LS_STV0 positive power supply. Pls refer to function block and application circuit.
10	VGH1	P	LS_VGL, LS_LVGL, CLK1 to 12, and LS_STV1A/1B positive power supply. Refer to function block and application circuit.
11	TERMINATE	I	Level shifter input signal. Pull CLK1 to 12 low on TERMINATE level trigger.
12	STV0	I	Level Shifter input signal (GOA reset signal) rising/falling edge trigger.
13	STV1B	I	Level Shifter input signal (start pulse for GOA) rising/falling edge trigger.
14	STV1A	I	Level Shifter input signal (start pulse for GOA) rising/falling edge trigger.
15, 16	NC	--	
17	CPV2	I	Level shifter input signal rising/falling edge trigger.
18	CPV1	I	Level shifter input signal rising/falling edge trigger.
19	LC	I	Level shifter input signal (low frequency clock).
20	DVDD	P	Supply voltage input.
21	DIS_SENSE	I	Level shifter input discharge sensing voltage
22	FAULT	O	FAULT terminal
23	A0	I	Slave address assignment
24	SDA	I/O	I2C - Compatible serial bidirectional data line
25	SCL	I	I2C - Compatible clock input
26, 41	GND	--	Ground. The exposed pad (pin41) must be soldered to a large PCB and connected to GND for maximum dissipation.
27	LVGL	P	LS_LVGL, CLK1 to 12, LS_STV0/STV1A/STV1B and VDDE/VDDO negative power supply. Please refer to function block and application circuit.(The voltage of LVGL must be lower (or equal) than VGL).
28	VGL	P	Low level of LS_VGL circuit. Please refer to the function and the application circuit

29	LS_VGL	O	Discharge function for liquid crystal capacitor
30	RCS	O	GPM rising/falling slope setting.
31	CLK12	O	Level shifter output.
32	CLK11	O	Level shifter output.
33	CLK10	O	Level shifter output.
34	CLK9	O	Level shifter output.
35	CLK8	O	Level shifter output.
36	CLK7	O	Level shifter output.
37	CLK6	O	Level shifter output.
38	CLK5	O	Level shifter output.
39	CLK4	O	Level shifter output.
40	CLK3	O	Level shifter output.

THEORY OF OPERATION

General Description

The iML7276 provides 19-channel Level Shifter designed to drive the GOA panel. This device converts the logic-level signals generated by the Timing Controller (TCON) to high-level signals required by GOA panel.

Power On Sequence

When the DVDD exceeds UVLO, the internal signal ENA for condensed GOA logic will be high. The outputs of Level Shifter CLK1~CLK12, LS_LVGL should follow LVGL level since DVDD exceeds UVLO. The outputs of Level Shifter LS_STV0, LS_STV1A and LS_STV1B should follow LVGL level since VDD exceeds UVLO. The outputs of Level Shifter VDDE and VDDO should follow LC transient one VGH2 the other LVGL since VDD exceeds UVLO. After exceeds DVDD UVLO rising, CLK1 to CLK12 do not output until receiving the first STV1A/1B rising edge. After DVDD>DVDD_UVLO rising and LC rising edge, VDDE and VDDO will follow LC truth table transient.

LC Truth Table		
LC(from TCON)	0	1
VDDE	0	1
VDDO	1	0

According to GOA circuit experience, it is recommended that 1. VDDE and VDDO start to work earlier than the 1st STV1A/1B by 28us; 2. Logic signal (STV0/STV1A/STV1B, LC, CPV1 to 4) must be sent after VGH power ready.
The recommended power-on sequence is DVDD (2.6 to 5.5V) → LVGL → VGL → VGH1/2 or VDD (2.6 to 5.5V) → LVGL=VGL → VGH1/2.
The concern of IC design is focus on VGL and LVGL ESD diode. The most negative voltage must be ready before the other negative voltage.

Power Sequence

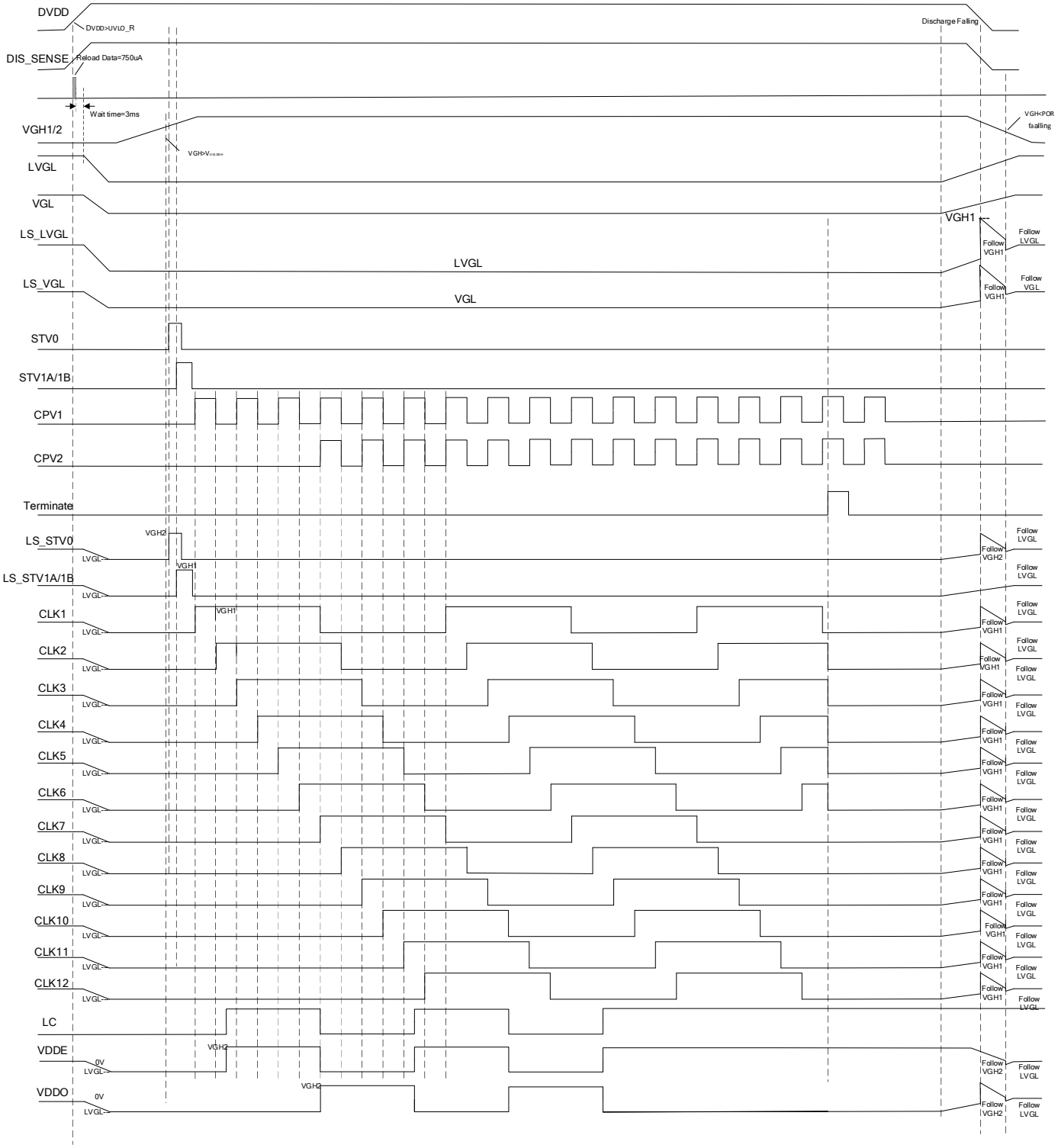


Figure 2. The IML7276 Power Sequence

Table 1 Power On (from 0 to DVDD) Condition

Case	Analog Power Input			Logic Input				Analog Output					
	DVDD	DIS_SENSE	VGH	STV0	STV1A/1B	CPV1~2	LC	LS_STV0	LS_STV1A/1B	CLK	VDDE/VDDO	LS_VGL	LS_LVGL
1.1	<UVLO	Don't Care	<POR	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	LVGL	VGL	LVGL
1.2	<UVLO	Don't Care	>POR&<UVLO	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	Hi-Z	VGL	LVGL
1.3	<UVLO	Don't Care	>UVLO	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	Hi-Z	VGL	LVGL
1.4	>UVLO	Don't Care	>POR&<UVLO	Don't Care	Don't Care	Don't Care	w/o signal	LVGL	LVGL	LVGL	LVGL※1	VGL	LVGL
1.5	>UVLO	Don't Care	>POR&<UVLO	Don't Care	Don't Care	Don't Care	w/I signal	LVGL	LVGL	LVGL	LVGL※1	VGL	LVGL
1.6	>UVLO	<Threshold	>UVLO	Don't Care	Don't Care	Don't Care	w/o signal	LVGL	LVGL	LVGL	LVGL※1	VGL	LVGL
1.7	>UVLO	<Threshold	>UVLO	Don't Care	Don't Care	Don't Care	w/I signal	LVGL	LVGL	LVGL	LVGL※1	VGL	LVGL
2.1	>UVLO	>Threshold	>UVLO	w/o signal	w/I signal	w/I signal	w/o signal	LVGL	Normal	LVGL	LVGL※1	VGL	LVGL
2.2	>UVLO	>Threshold	>UVLO	w/I signal	w/o signal	w/I signal	w/o signal	Normal	LVGL	LVGL	LVGL※1	VGL	LVGL
2.3	>UVLO	>Threshold	>UVLO	w/o signal	w/I signal	w/I signal	w/I signal	LVGL	Normal	LVGL	VDDE=LC_IN VDDO=VDDE_B	VGL	LVGL
2.4	>UVLO	>Threshold	>UVLO	w/I signal	w/o signal	w/o signal	w/I signal	Normal	LVGL	LVGL	VDDE=LC_IN VDDO=VDDE_B	VGL	LVGL
3.1	>UVLO	>Threshold	>UVLO	w/I signal	w/I signal	w/I signal	w/I signal	Normal	Normal	Normal	VDDE=LC_IN VDDO=VDDE_B	VGL	LVGL

Table 2 Power Off(from DVDD to 0) Condition

Case	Analog Power Input			Logic Input				Analog Output					
	DVDD	DIS_SENSE	VGH	STV0	STV1A/1B	CPV1~2	LC	LS_STV0	LS_STV1A/1B	CLK	VDDE/VDDO	LS_VGL	LS_LVGL
1	>UVLO	<Threshold	>UVLO	Don't Care	Don't Care	Don't Care	Don't Care	LVGL※2	LVGL※3	VGH1※4	VGH2※4	VGH1	LVGL※5
2	<UVLO	Don't Care	>UVLO	Don't Care	Don't Care	Don't Care	Don't Care	LVGL※2	LVGL※3	VGH1※4	VGH2※4	VGH1	LVGL※5
3	<UVLO	Don't Care	<UVLO&>POR	Don't Care	Don't Care	Don't Care	Don't Care	LVGL※2	LVGL※3	VGH1※4	VGH2※4	VGH1	LVGL※5
4	<UVLO	Don't Care	<POR	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	LVGL	VGL	LVGL
5	>UVLO	>Threshold	<UVLO&>POR	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	LVGL	VGL	LVGL

Notes:

(1) ※1 : For VDDE/VDDO Initial state. Select LVGL or VGH2 by 04h[7:6]

(2) ※2 : For LS_STV0 Discharge state. Select LVGL or VGH2 by 03h[7]

(3) ※3 : For LS_STV1A/1B Discharge state. Select LVGL or VGH1 by 03h[6]

(4) ※4 : For CLKx and VDDE/VDDO Discharge state. Select LVGL or VGH1/2 by 03h[5]

(5) ※5 : For LS_LVGL Discharge state. Select LVGL or VGH1 by 03h[4]

Protection

The iML7276 contains Over-Temperature Protection (OTP), Over-Current Protection (OCP). The following table shows the main behavior of each protection.

Table 3. Over temperature Protection and Over Current Protections

Function / Protection	Output	FAULT	Recovery
OTP	Hi-Z	Pull low	TJ decrease 20°C(Typ.)
OCP	Hi-Z	Pull low	(DVDD < VUVLO) & [VGH < UVLO falling]

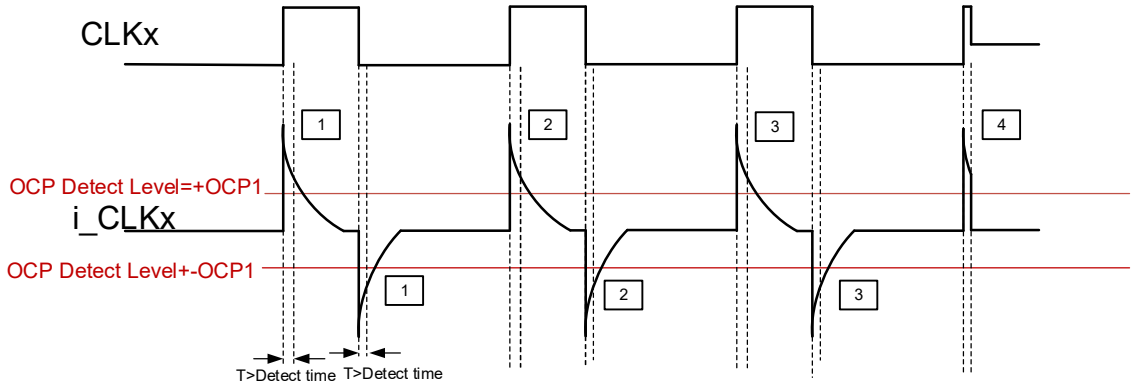
Over-Temperature Protection (OTP)

An Over-Temperature Protection (OTP) is equipped to prevent iML7276 from overheating due to the excessive power dissipation. The OTP will stop operating while junction temperature exceeds 150°C (Min.). All of output channel start operating while the decrease of junction temperature approximately 20°C (Typ.).

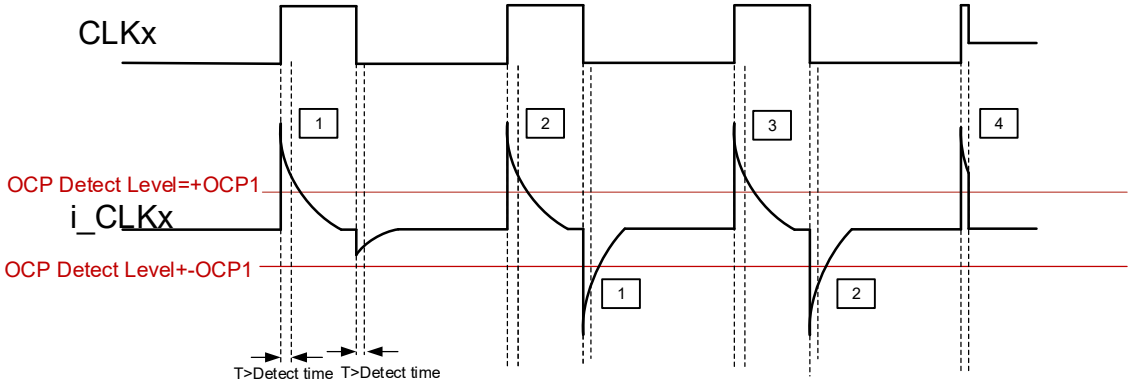
Over-Current Protection (OCP)

The iML7276 can detect output pins (LS_STV0/1A/1B, CLK1 to 12, VDDE, VDDO, LS_LVGL, and LS_VGL) short to each other short current. If the pin to pin short current over limit, the IC all outputs (STV0/1A/1B, CLK1 to 12, VDDE, VDDO, DIS_LVGL, and LS_VGL) will pull high impendence state. After VUVLO and VGH <POR falling, IC recovers again.

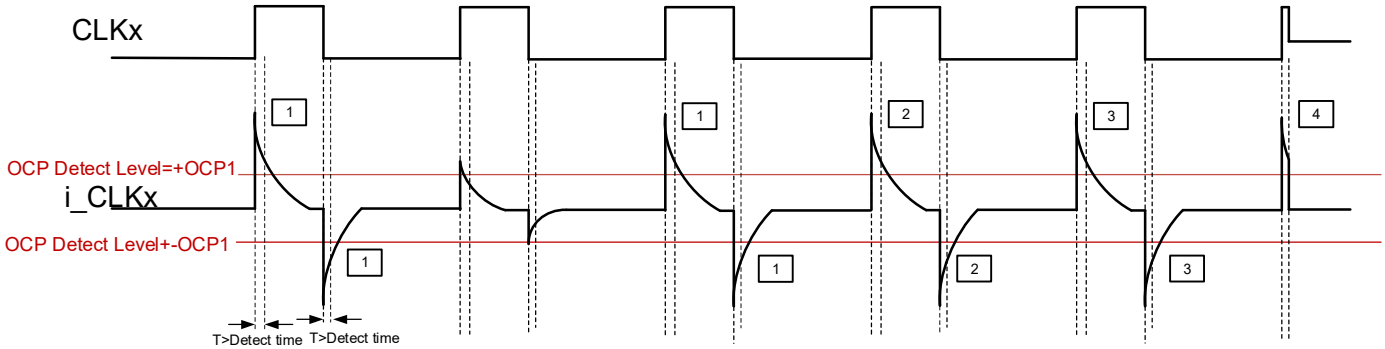
CLKx OCP case1



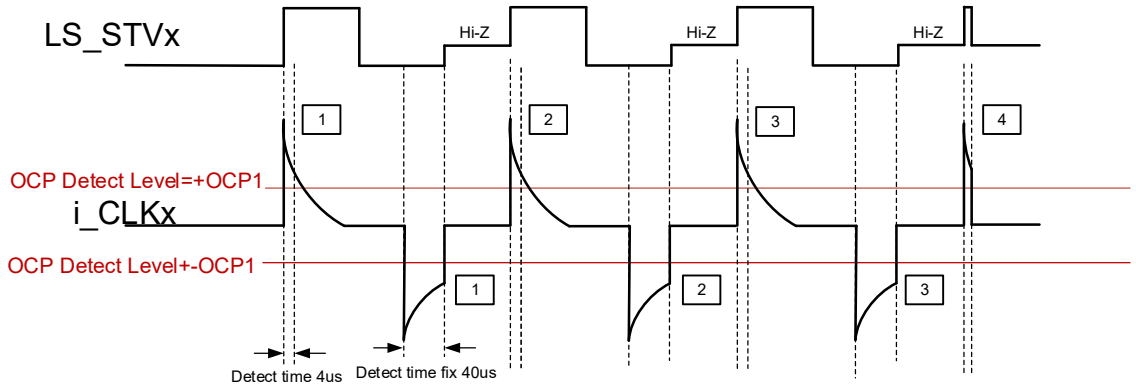
CLKx OCP case2



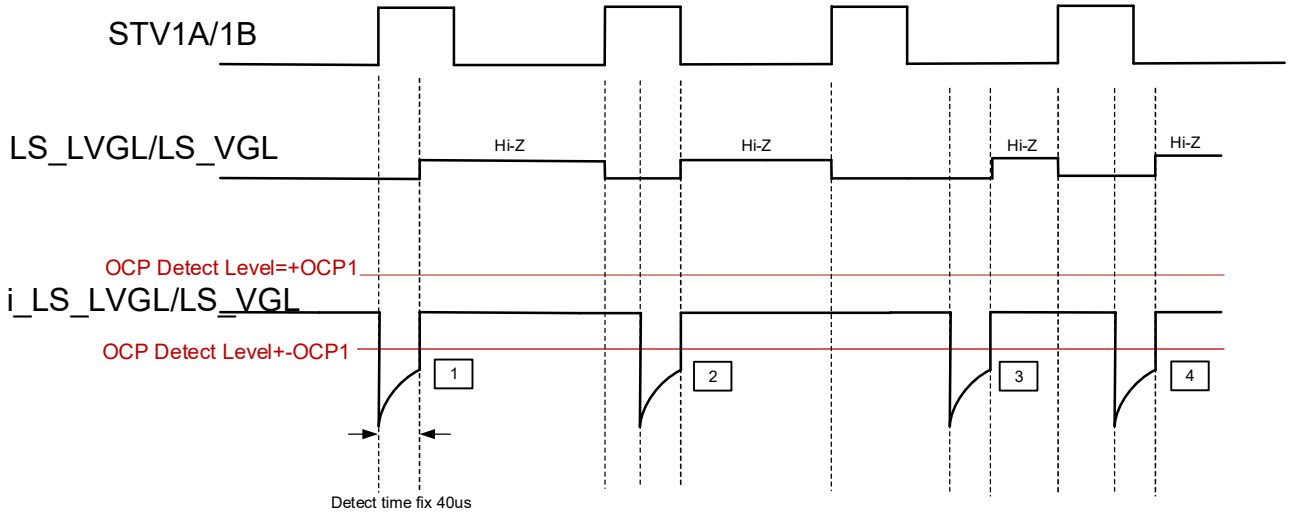
CLKx OCP case3



LS_STV OCP case4



LS_LVGL/LS_VGL OCP case5



VDDE/VDDO OCP case6

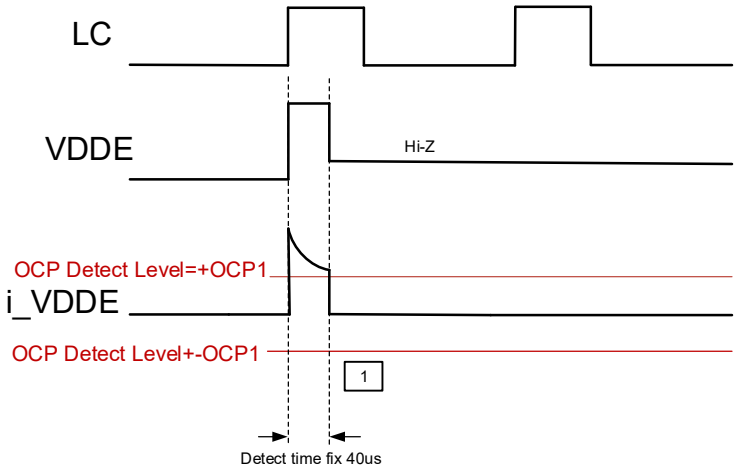


Figure 4. OCP Detection Waveforms

IC FAULT Function

During normal operating, FAULT pin becomes high-state. OTP or OCP happen, the FAULT pin becomes low-state and and each output channel becomes Hi-Z.

Timing Diagram

12CLK:
Phase=Reg00h[7:5]=100b to 111b
Reg03h[0]=0b or 1b

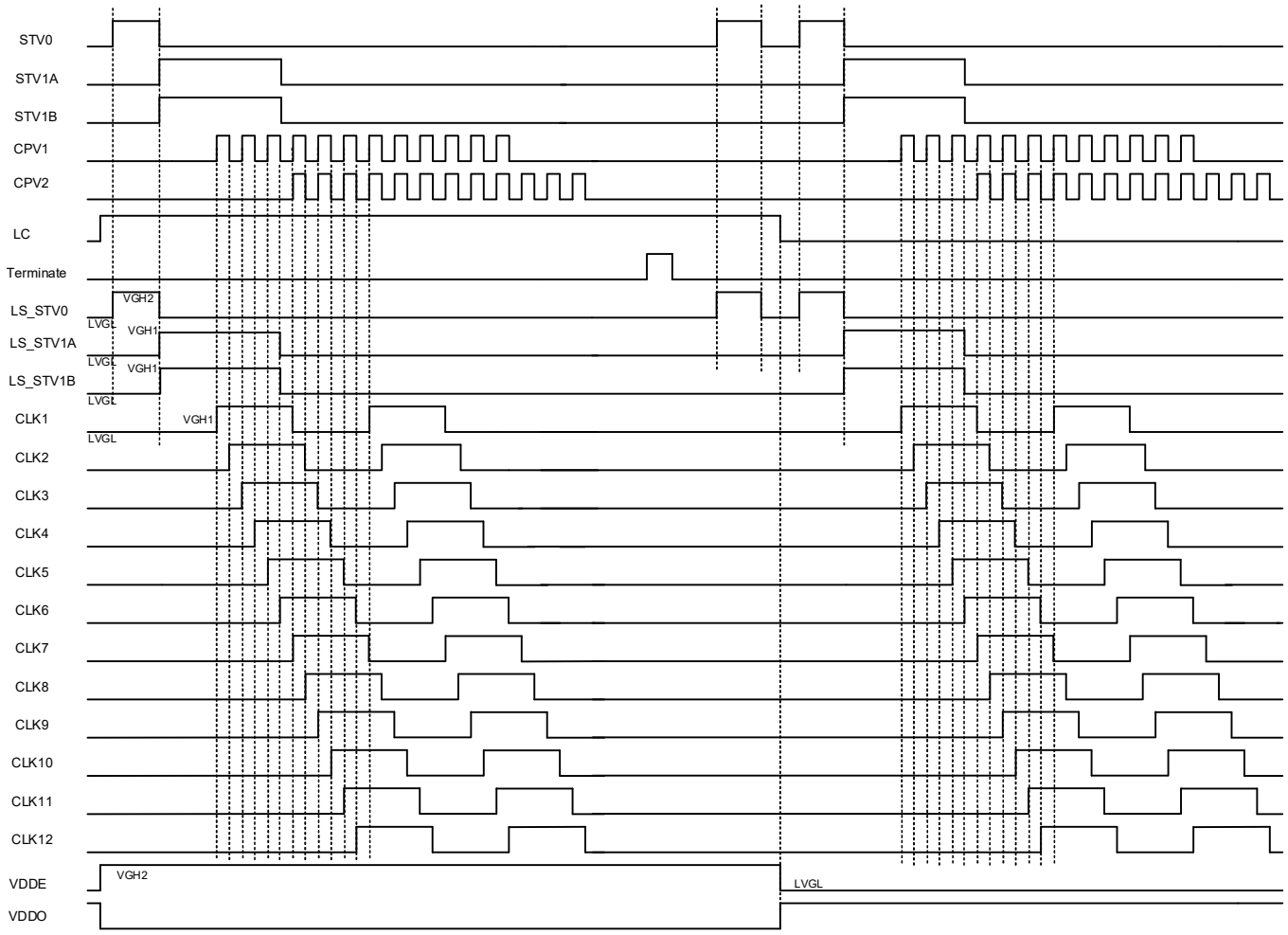


Figure 5. 12CLK Timing Diagram 1

12CLK:
Phase=Reg00h[7:5]=100b to 111b
Reg03h[0]=0b

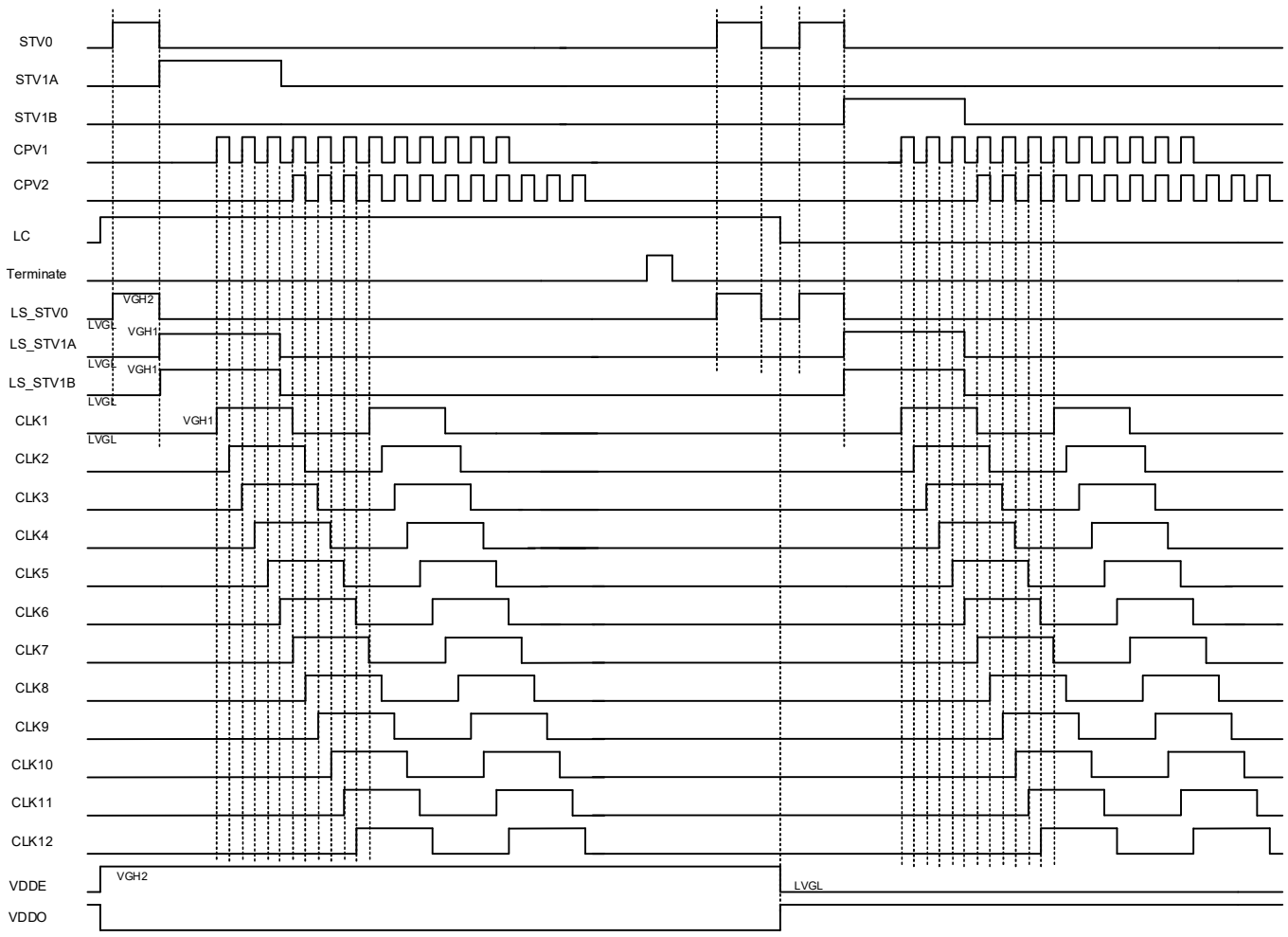


Figure 6. 12CLK Timing Diagram 2

12CLK:
Phase=Reg00h[7:5]=100b to 111b
Reg03h[0]=1b

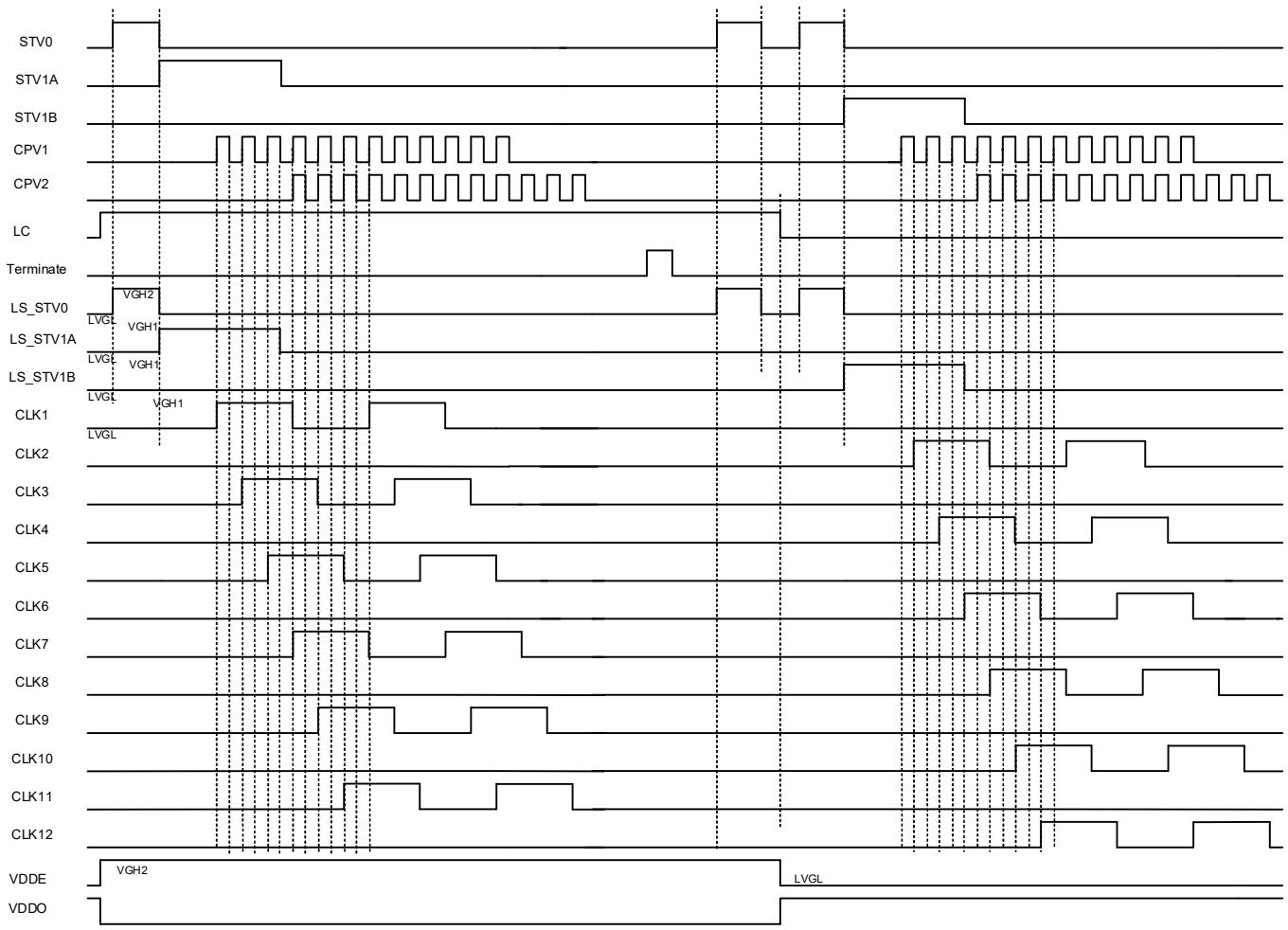
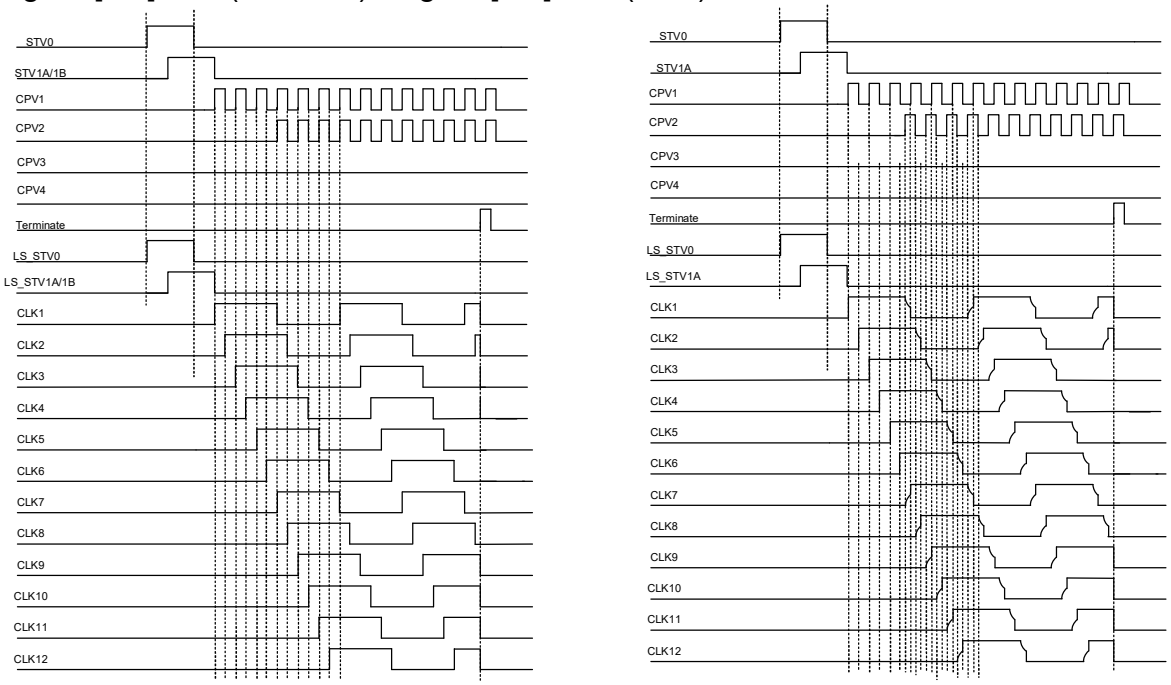


Figure 7. 12CLK Timing Diagram 3

GPM Function

Reg03h[3:2]=00b(disabled)/Reg03h[3:2]=01b(both)



Reg03h[3:2]=10b(rising)/Reg03h[3:2]=11b(falling)

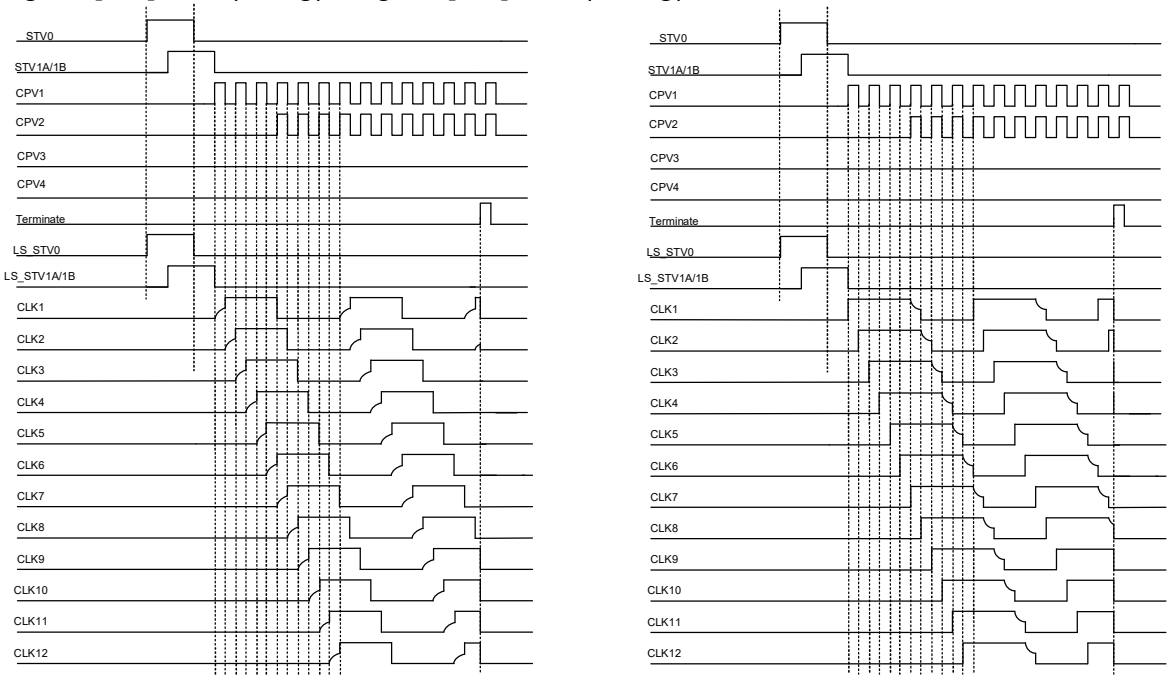


Figure 8. GPM_2CPV

Terminate Mode

Reg00h[4]=0b/Reg00h[4]=1b

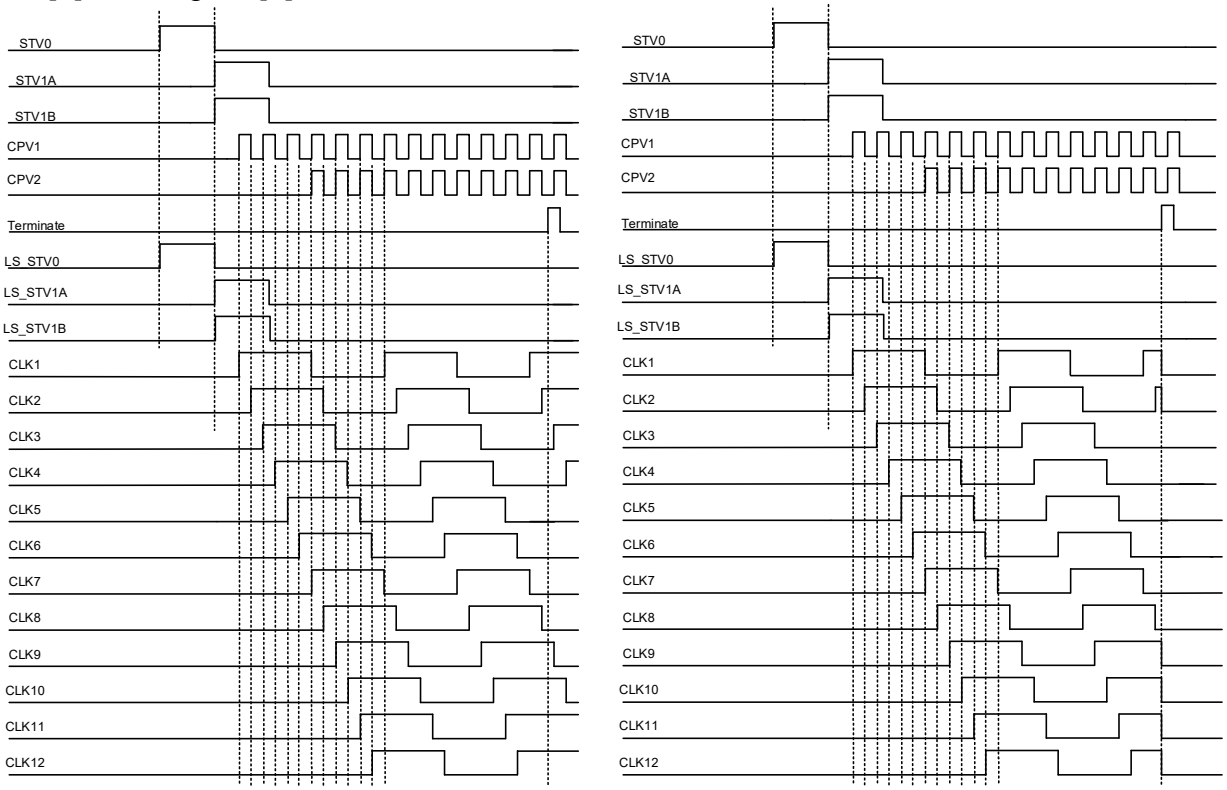
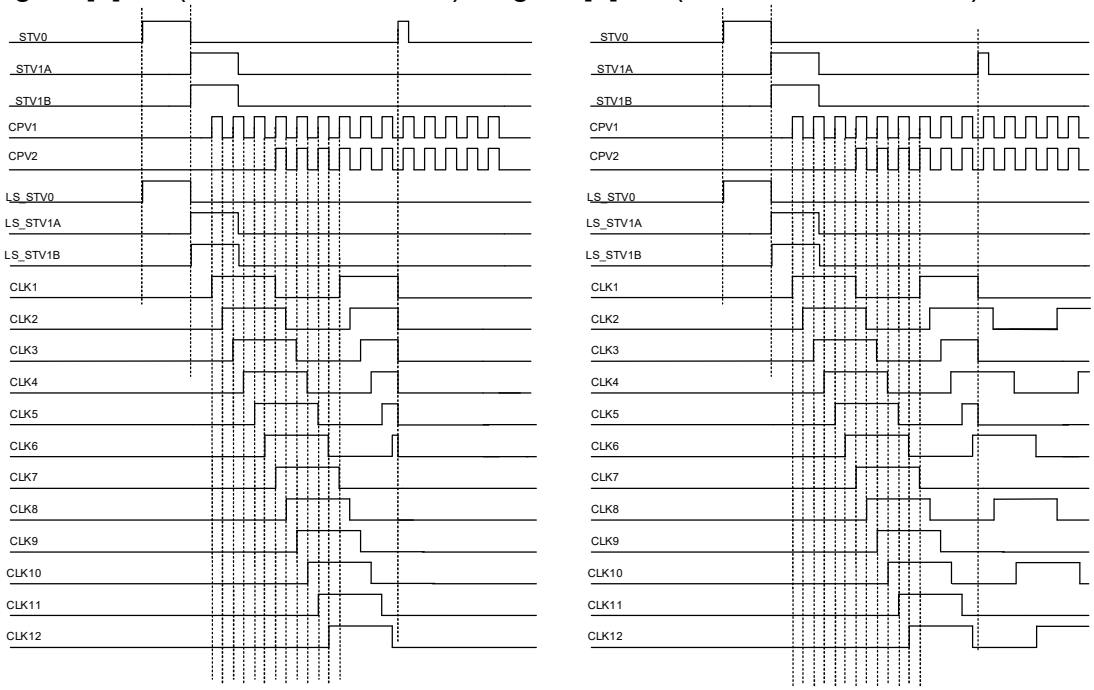


Figure 9. Terminate Mode

STVx Reset Function

Reg01h[2]=1b(STV0 reset enable)/Reg01h[1]=1b(STV1A reset enable)



Reg01h[1]=1b(STV1B reset enable)

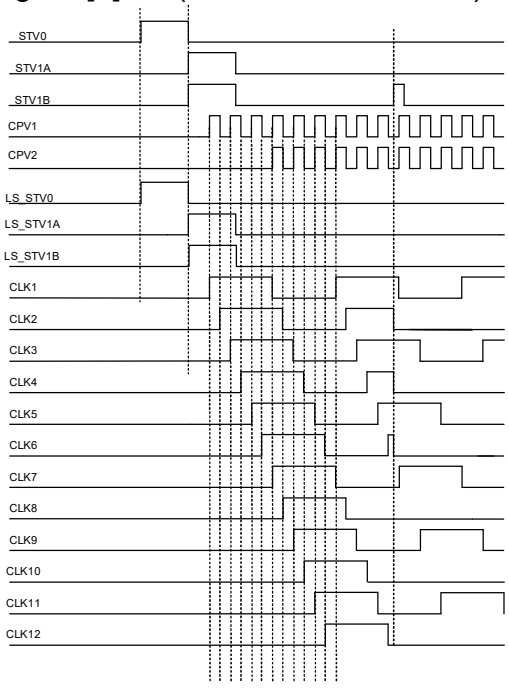


Figure 10. STVx Reset Function

I²C Serial Interface

The iML7276 uses two wires, serial data (SDA) and serial clock (SCL), to communicate. They are connected via the resistors to an external positive power supply voltage. This means that when the bus is free, both lines are high. The device on the bus has open-drain pins. Each device on the I²C bus responds to a slave address byte sent immediately following a Start Condition. Figure 8 shows the definition of timing on I²C bus.

The slave address byte contains the slave address in the most significant 7 bits and the R/W bit in the least significant bit. The iML7276 consist of slave address. Table 4 shows the slave address.

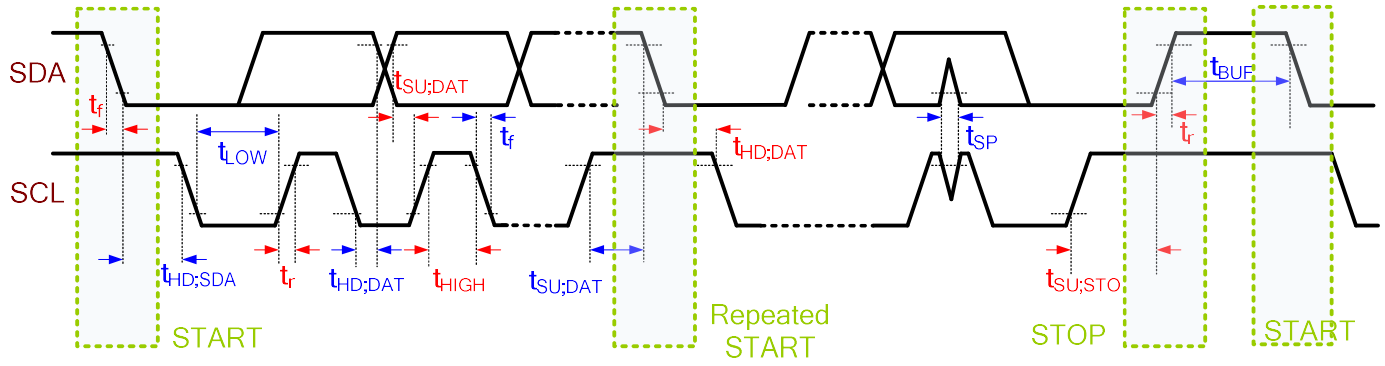


Table 4. Slave Address byte

Bit	7	6	5	4	3	2	1	LSB
Data	0	1	0	1	0	0	A0	R / $\overline{W}$

Memory of the iML7276

The iML7276 has two types of memory. One type is non-volatile EEPROM and the other is volatile register memory. The EEPROM stores all register code values for the iML7276 even when the chip is not powered. When the chip is powered up, all code values of the EEPROM are automatically copied into the volatile register memory. The volatile register memory can be written or read through I²C at any time.

Write/Read Data to/from the iML7276

Write operation One 8-bit data value is written into the register by each I²C WRITE operation. A write to the iML7276 consists of START condition, the slave address of iML7276 with R/W bit set to 0, the memory address, 8bits of data, and STOP condition.

A special command code, writing Reg05h=A5h by I²C WRITE operation, makes writing all register code data into the internal EEPROM. A special command code, writing Reg05h=A4h by I²C WRITE operation, makes all NVM data downloaded to the register. X is decided by A0 pin.

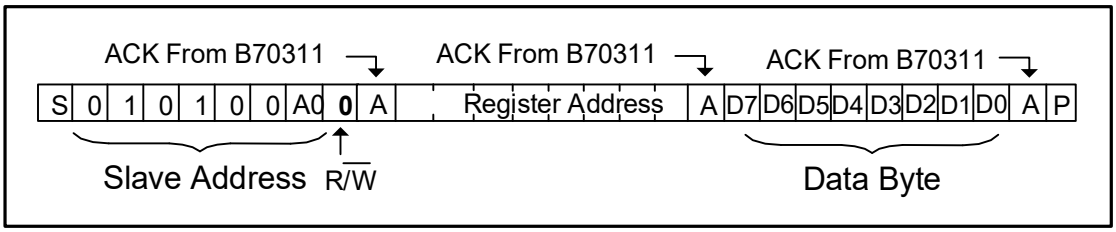


Figure 11. Writing to the single DAC register

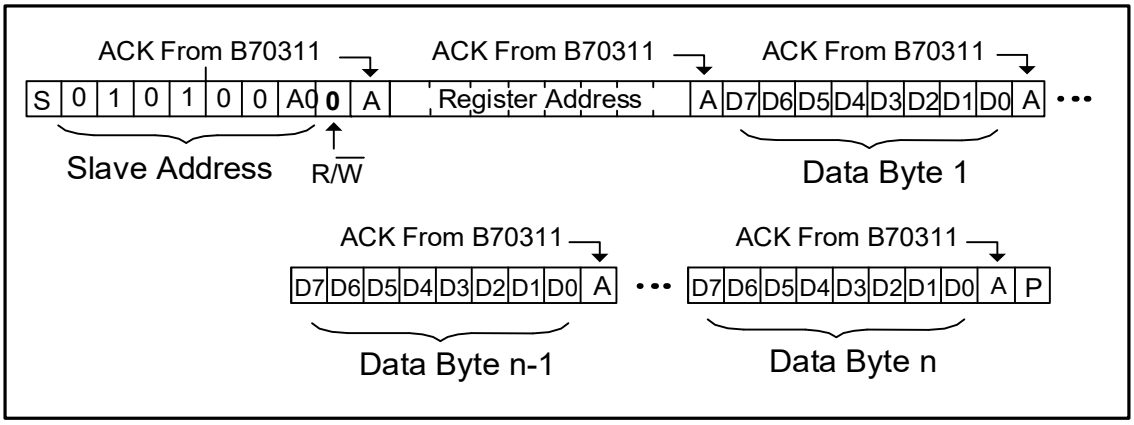


Figure 12. Writing to the multiple registers

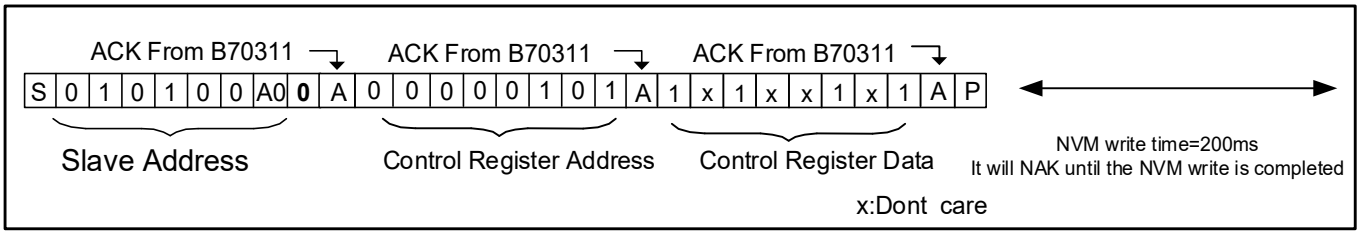


Figure 13. Writing all register data to NVM

Read operation One 8-bit data value is read from the register by each I²C READ operation. The stored data on the EEPROM is not directly accessible during a normal read operation. All EEPROM data is copied into register memory whenever the power is newly on, or the special command of Reg05h=A4h by I2C. If another 8-bits of data needs to be read, a new memory address must be written by a new I²C READ operation. Consecutive data reads without writing a memory address is not allowed.

A read from the iML7276 consists of START condition, the slave address of iML7276 with R/W bit set to 0, the memory address, repeated START condition, and the slave address of iML7276 with R/W bit set to 1. Then the iML7276 transmits the contents of the register memory. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). A STOP condition can be issued after reading one data byte.

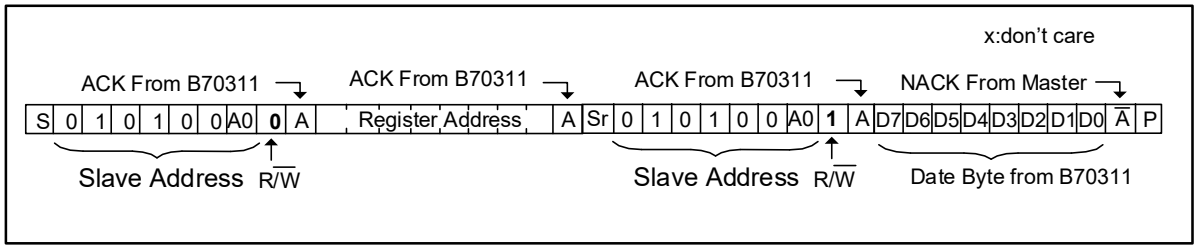


Figure 14. Reading from the single DAC register

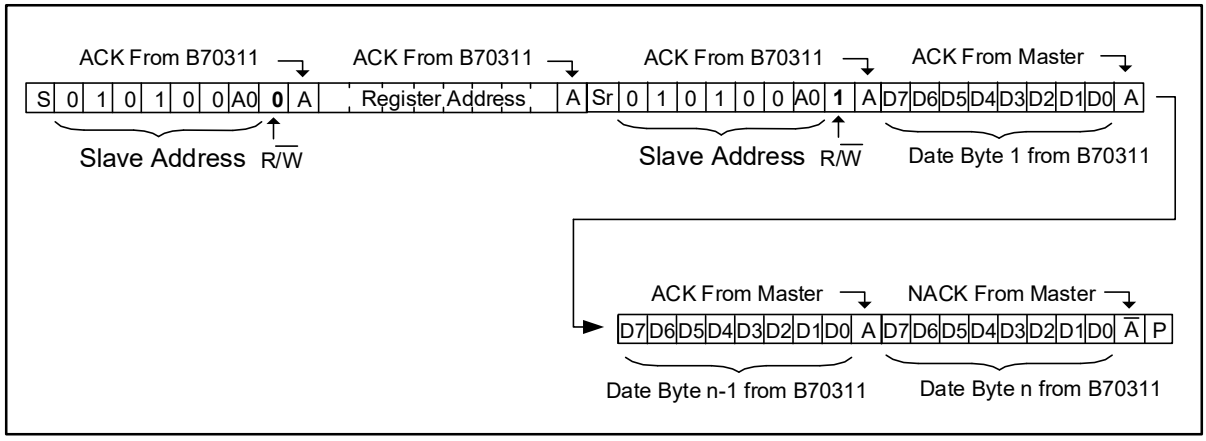


Figure 15. Reading from the multiple DAC registers

Register Map

Reg	Name	Description	Default Value	Range	Note
00h	SEL_PHASE	[7:5] Phase SEL	100b: 12Phase	000b: 4Phase 001b: 6Phase 010b: 8Phase 011b: 10Phase 100b~111b: 12Phase	
	TERM_Mode	[4] TERM_MODE	1b	0b: When terminate signal rising comes, CLK won't be turned to LVGL. 1b: All CLK pulled low while terminate rising signal comes.	
	CLK Slew Rate	[3:2] CLK Slew Rate	01b: 1000V/us	00b: 1500V/us, 01b: 1000V/us, 10b: 500V/us, 11b: 100V/us	
	DIS_SENSE	[1:0] DIS_SENSE	11b: 0.8V	00b: 1.8V(UVLOF) 01b: 2.3V 10b: 2.7V 11b: 0.8V	
01h	LS_STV/LS_VGL/LS_LVGL OCP_COUNT	[7:6] LS_STV/LS_VGL/LS_LVGL OCP_COUNT	0b: 4 times	00b: 4 times 01b: 8 times 10b: 16 times 11b: 32 times	Continuous Trigger
	LS_STV/VDDE/VDDO/LS_VGL/LS_LVGL OCP LEVEL	[5:3] LS_STV/VDDE/VDDO/LS_VGL/LS_LVGL OCP LEVEL	100b: 70mA	000b: disable 001b: 20mA 010b: 30mA 011b: 50mA 100b: 70mA 101b: 90mA 110b: 120mA 111b: 160mA	
	STV0_RESET	[2] STV0_RESET	1b	0b: Don't reset anything 1b: Reset CLKx to LVGL	
	STV1A/1B_RESET	[1] STV1A/1B_RESET	1b	0b: Don't reset anything 1b: Reset CLKx to LVGL	
	Reserved	[0]	0b		2CPV input: NVM should be written to 1b Others(4CPV input): keeps 0b
02h	CLK_OCP_COUNT	[7:6] CLK_OCP_COUNT	00b: 4 times	00b: 4 times 01b: 8 times 10b: 16 times 11b: 32 times	Continuous Trigger
	CLK_OCP_LEVEL	[5:3] CLK_OCP_LEVEL	100b: 70mA	000b: Disable 001b: 20mA 010b: 30mA 011b: 50mA 100b: 70mA 101b: 90mA 110b: 120mA 111b: 160mA	-
	CLK/STV_OCP_DET_TIME	[2:0] CLK/STV_OCP_DET_TIM	011b: 3 us	000b: 0.5us 001b: 1us	

		E		010b: 2us 011b: 3us 100b: 4us 101b: 6us 110b: 7us 111b: 8us	
03h	DIS_STV0_SEL	[7] DIS_STV0_SEL	0b: Pull to LVGL	0b: Pull to LVGL 1b: Pull to VGH2	
	DIS_STV1A/1B_SEL	[6] DIS_STV1A/1B_SEL	0b: Pull to LVGL	0b: Pull to LVGL 1b: Pull to VGH1	
	DIS_CLK_VDDE/VDDO_SEL	[5] DIS_CLK_VDDE/VDDO_SEL	1b: CLK Pull to VGH1 VDDE/VDDO Pull to VGH2	0b: Pull to LVGL 1b: CLK Pull to VGH1 VDDE/VDDO Pull to VGH2	
	LS_LVGL_SEL	[4] LS_LVGL_SEL	0b: Pull to LVGL	0b: Pull to LVGL 1b: Pull to VGH1	
	CS MODE/GPMSE OPTION	[3:2] CS MODE/GPM SE OPTION	00b: CS/GPM OFF	00b: CS/GPM OFF 01b: CS ON 10b: GPM Rising 11b: GPM Falling	
	VGH_UVLO_R	[1] VGH_UVLO_R	1b: 15V	0b: 8V 1b: 15V	
	STV1A/1B CLK CTRL	[0] STV1A/1B CLK CTRL	1b: ON	0b: OFF 1b: ON: STV1A and 1B can control CLK1/3/5/7/9/11 and CLK2/4/6/8/10 respectively.	
04h	VDDE/VDDO INITIAL_STATE	[7:6] VDDE/VDDO INITIAL_STATE	10b: VDDE Pull to VGH2, VDDO Pull to LVGL	00b: Both Pull to LVGL 01b: VDDE Pull to LVGL VDDO Pull to VGH2 10b: VDDE Pull to VGH2 VDDO Pull to LVGL 11b: Both Pull to VGH2	-
	Reserved	[5:3]	000b		NVM should keep 000b
	DUAL LINE EN	[2] DUAL LINE EN	0b: OFF	0b: OFF 1b: ON	
	Reserved	[1:0]	00b	.	Read Only
05h	Control Byte	0x00 = A5 → WR Register Data to NVM (0x00h to 0x04h) 0x00 = A4 → Download NVM to Register (0x00h to 0x04h)			Write only Register (Non NVM)

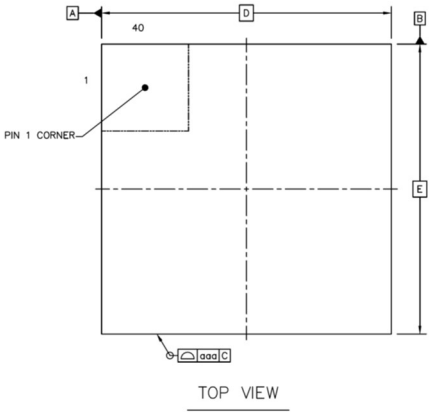
Register Details

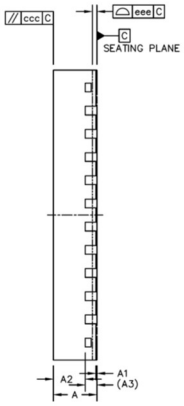
Control register Set (0x05)

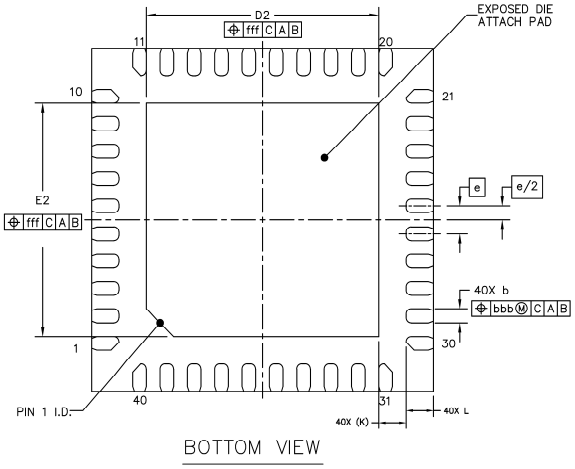
The Non-Volatile Memory (NVM) will be written to or read from via the Control Register.
The control register is a register only (cannot be written into EEPROM)

Name	Bit	Access	Default	Description
Control Reg 0x00	7	W	0	0x00 = A5 → WR Register Data to NVM (0x00h to 0x04h) 0x00 = A4 → Download NVM to Register (0x00h to 0x04h)
	6		0	
	5		0	
	4		0	
	3		0	
	2		0	
	1		0	
	0		0	

PACKAGE INFORMATION [Drawing is not to scale]







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	3.3	3.4	3.5
	Y	E2	3.3	3.4	3.5
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.4 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	