Features

- 2.5 A maximum peak output current
- Drive IGBTs up to I_C = 150 A, V_{CE} = 1200 V
- Optically isolated, FAULT status feedback
- I_{DD}(MAX) < 5mA maximum pulse width distortion (PWD)
- CMOS/TTL compatible
- 500 ns maximum propagation delay over temperature range
- “Soft” IGBT turn-off
- Integrated fail-safe IGBT protection
- —Desat (V_{CE}) detection
- —Under Voltage Lock-Out protection (UVLO)
- Wide operating V_{CC} range: 15 to 30 Volts
- -40°C to +110°C operating temperature range
- 15 kV/μs min. Common Mode Rejection (C_{MR}) at V_{CM} = 1500V

Applications

- Isolated IGBT/Power MOSFET gate drive
- AC and brushless DC motor drive
- Industrial inverter
- Induction heating
- Switch Mode Power Supply (SMPS)
- Uninterruptible power supply (UPS)

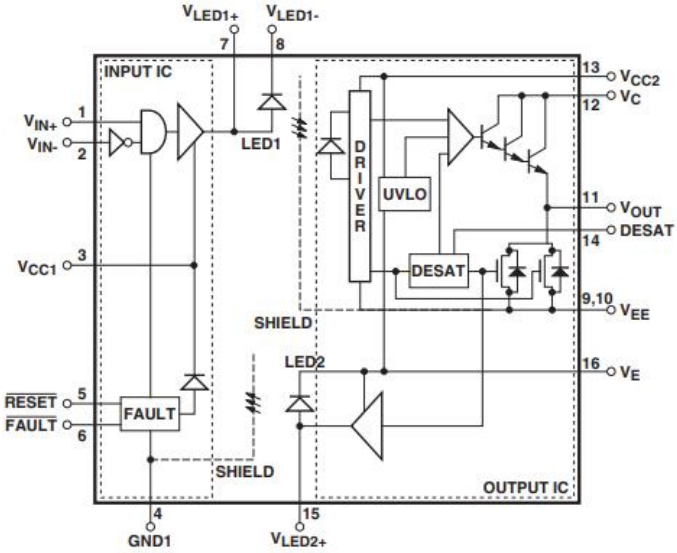
Caution

It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Description

The ICPL-316J is a highly integrated power control device that incorporates all the necessary components for a complete, isolated IGBT gate drive circuit with fault protection and feedback into one SOP-16 package.

TTL input logic levels allow direct interface with a microcontroller, and an optically isolated power output stage drives IGBTs with power ratings of up to 150 A and 1200 V.An output IC provides local protection for the IGBT to prevent damage during overcurrents, and a second optical link provides a fully isolated fault status feedback signal for the microcontroller. A built in “watchdog” circuit monitors the power stage supply voltage to prevent IGBT caused by insufficient gate drive voltages. This integrated IGBT gate driver is designed to increase the performance and reliability of a motor drive.



ORDERING INFORMATION

Outline	Part Number	Package	Marking	Packing	Packing Size	Quantity
	ICPL-316J-500E	SOP16	ICPL 316J /YYWW B	Reel	13 "	850

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CONTENTS

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PIN CONFIGURATION AND FUNCTIONS

Pin	Symbol	Description
1	V_{IN+}	Noninverting gate drive voltage output (VOUT) control input
2	V_{IN-}	Inverting gate drive voltage output (VOUT) control input
3	V_{CC1}	Positive input supply voltage. (4.5 V to 5.5 V)
4	GND1	Input Ground
5	$\overline{\text{RESET}}$	$\overline{\text{FAULT}}$ reset input. A logic low input for at least 0.1 µs, asynchronously resets $\overline{\text{FAULT}}$ output high and enables VIN. Synchronous control of $\overline{\text{RESET}}$ relative to VIN is required. $\overline{\text{RESET}}$ is not affected by UVLO. Asserting $\overline{\text{RESET}}$ while VOUT is high does not affect VOUT.
6	$\overline{\text{FAULT}}$	Fault output. $\overline{\text{FAULT}}$ changes from a high impedance state to a logic low output within 5 µs of the voltage on the DESAT pin exceeding an internal reference voltage of 7V. $\overline{\text{FAULT}}$ output remains low until RESET is brought low.$\overline{\text{FAULT}}$ output is an open collector which allows the FAULT outputs from all ICPL-316Js in a circuit to be connected together in a “wired OR” forming a single fault bus for interfacing directly to the micro-controller.
7	V_{LED1+}	LED 1 anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only.)
8	V_{LED1-}	LED 1 cathode. This pin must be connected to ground.
9	V_{EE}	Output supply voltage
10	V_{EE}	Output supply voltage
11	V_{OUT}	Gate drive voltage output
12	V_C	Positive output supply voltage
13	V_{CC2}	Positive output supply voltage
14	DESAT	Desaturation voltage input. When the voltage on DESAT exceeds an internal reference voltage of 7V while the IGBT is on, FAULT output is changed from a high impedance state to a logic low state within 5 µs.
15	V_{LED2+}	LED2 anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only.)
16	V_E	Common (IGBT emitter) output supply voltage

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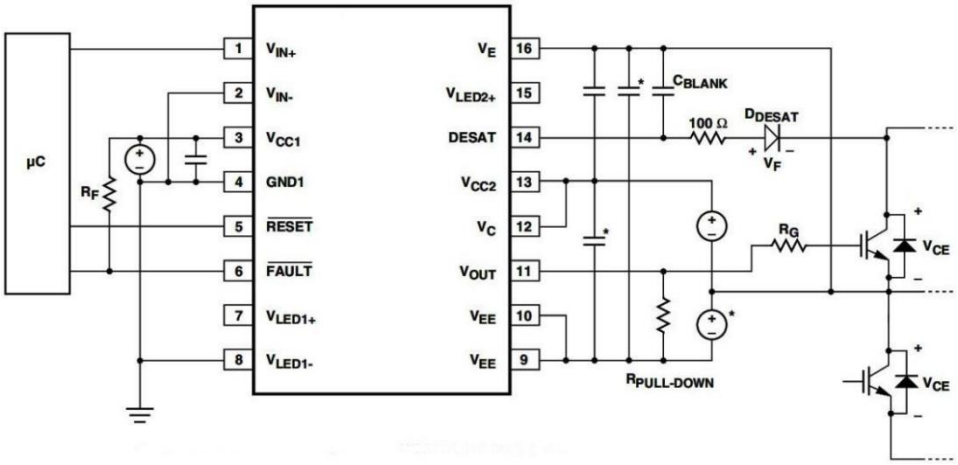
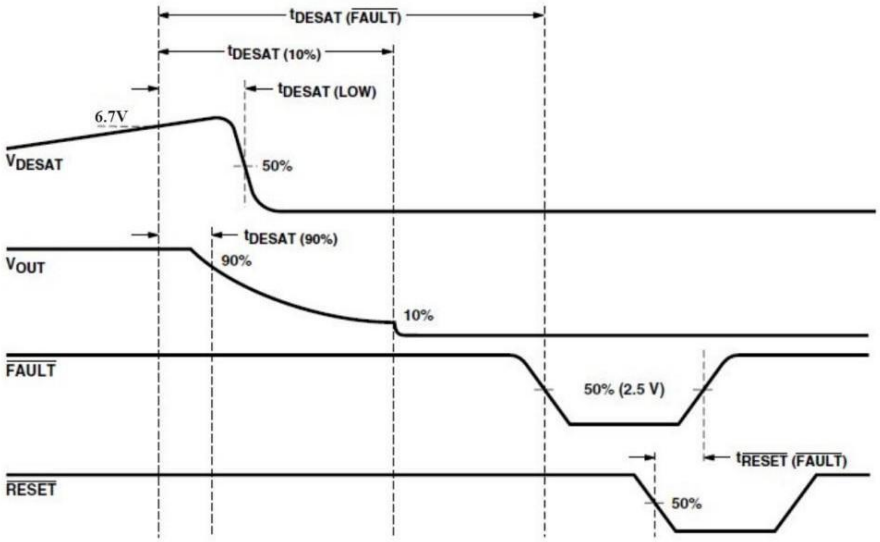
Typical Fault Protected IGBT Gate Drive Circuit

The ICPL-316J is an easy-to use, intelligent gate driver which makes IGBT VCE fault protection compact, affordable, and easy-to- implement. Features such as user configurable inputs, integrated VCE detection, under voltage lockout (UVLO), soft IGBT turn-off and isolated fault feedback provide maximum design flexibility and circuit protection



Description of Operation



Description of Operation during Fault Condition

1. DESAT terminalmonitors the IGBT V_{CE} voltage through DESAT
2. When the voltage on the DESAT terminal exceeds 7 volts, the IGBT gate voltage (V_{OUT}) is slowly lowered
3. FAULT output goes low, notifying the microcontroller of the fault condition
4. Microcontroller takes appropriate action

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OUTPUT CONTROL

The outputs (V_{OUT} and FAULT) of the ICPL-316J are controlled by the combination of V_{IN}, UVLO and a detected IGBT Desat condition. As indicated in the below table, the ICPL-316J can be configured as inverting or non-inverting using the V_{IN}+ or V_{IN}- inputs respectively. When an inverting configuration is desired, V_{IN}+ must be held high and V_{IN}- toggled. When a non-inverting configuration is desired, V_{IN}- must be held low and V_{IN}+ toggled. Once UVLO is not active (V_{CC2} - V_E > V_{UVLO}), V_{OUT} is allowed to go high, and the DESAT detection feature of the ICPL-316J will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once V_{UVLO+} > 11.6 V, DESAT will remain functional until V_{UVLO-} <12.4 V. Thus, the DESAT detection and UVLO features of the ICPL-316J work in conjunction to ensure constant IGBT protection.

Vinp	Vinn	Uvlo(Vdd2-Ve)	Desat Condition Detect	Fault	Vout
X	X	Active	X	X	Low
X	X	X	Yes	Low	Low
Low	X	X	X	X	Low
X	High	X	X	X	Low
High	Low	Not Active	No	High	High

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ABSOLUTE MAXIMUM RATINGS
（T_a=25℃unless otherwise specified）

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_s	-55	125	℃	-
Operating Temperature	T_a	-40	110		-
Output IC Junction Temperature	T_J	-40	125		1
Peak Output Current	$\|I_{o(peak)}\|$	-	2.5	A	2
Fault Output Current	$I_{\overline{FAULT}}$	-	10	mA	-
Positive Input Supply Voltage	V_{CC1}	-0.5	5.5	V	-
Input Pin Voltages	V_{IN}+, V_{IN-} and V_{RESET}	-0.5	5.5		-
Total Output Supply Voltage	(V_{CC2} - V_{EE})	-0.5	30		-
	T_a=90℃				-
Negative Output Supply Voltage	(V_E - V_{EE})	-0.5	15		3
Positive Output Supply Voltage	(V_{CC2} - V_E)	-0.5	35-(V_E -V_{EE})		-
Gate Drive Output Voltage	$V_{o(peak)}$	-0.5	V_{CC2}		-
Collector Voltage	V_C	V_{EE}+5V	V_{CC2}		-
DESAT Voltage	V_{DESAT}	V_E	V_E + 10		-
Output IC Power Dissipation	P_O	0	600	mW	1
Input IC Power Dissipation	P_I	0	150		

Note: This product is suitable for peak working voltage≤750V, RMS working voltage ≤ 400V.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max	Units	Note
Operating Temperature	T_a	-40	+110	°C	-
Input Supply Voltage	V_{CC1}	4.5	5.5	V	23
Total Output Supply Voltage	$(V_{CC2} - V_{EE})$	15	30		6
Negative Output Supply Voltage	$(V_E - V_{EE})$	-0.5	15		3
Positive Output Supply Voltage	$(V_{CC2} - V_E)$	-0.5	30 - $(V_E - V_{EE})$		-
Collector Voltage	V_C	V_{EE} + 6	V_{CC2}		-
Peak high-level output current	$\mid I_{OPH} \mid$	-	2.5	A	-
Peak low-level output current	$\mid I_{OPL} \mid$	-	2.5	A	-
DEST Voltage	V_{DESAT}	V_E	V_E+10	V	-
Output IC Power Dissipation	P_O	-	600	mW	-
Operating frequency	f	-	50	KHz	-

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ELECTRO-OPTICAL CHARACTERISTICS (DC)

Unless otherwise noted, all typical values at T_a = 25°C, V_{CC1} = 5V, and V_{CC2} - V_{EE} = 30V, V_E - V_{EE} = 0V； All Minimum/Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions	Fig	Note
Logic Low Input Voltages	V_{IN+L}, V_{IN-L} $V_{\overline{RESETL}}$	-	-	0.8	V	-	-	-
Logic High Input Voltages	V_{IN+H}, V_{IN-H} $V_{\overline{RESETH}}$	2.0	-	-		-	-	-
Logic Low Input Current	I_{IN+L}, I_{IN-L} $I_{\overline{RESETH}}$	-0.5	-0.4	-	mA	V_{IN}=0.4V	-	-
$\overline{FAULT}$ Logic Low Output Current	$I_{\overline{FAULTL}}$	5.0	12	-		V_{FAULT} =0.4V	27	-
$\overline{FAULT}$ Logic High Output Current	$I_{\overline{FAULTH}}$	-40		-	μA	V_{FAULT}=V_{CC1}	28	-
High Level Output Current	I_{OH}	-0.5	-1.5	-	A	V_{OUT}=V_{CC2} - 4 V	1, 6, 29	4
		-2.0	-	-		V_{OUT}=V_{CC2} -15 V		2
Low Level Output Current	I_{OL}	1.0	-	-		V_{OUT}=V_{EE}+1.5 V	2, 7, 30	4
		2.5	-	-		V_{OUT}=V_{EE}+4.0 V		2
Low Level Output Current During Fault Condition	I_{OLF}	90	140	230	mA	V_{OUT} - V_{EE}=14 V	3, 31	-
High Level Output Voltage	V_{OH}	V_C - 3.5	V_C - 2.5	V_C - 1.5	V	I_{OUT}= -100mA	4, 6, 32	5, 6, 7
		V_C -2.9	V_C - 2.0	V_C - 1.2		I_{OUT} = -650μA		
		-	-	V_C		I_{OUT} = 0	-	-
Low Level Output Voltage	V_{OL}	-	0.17	0.5		I_{OUT} = 100 mA	5, 7, 33	21
High Level Input Supply Current	I_{CC1H}	-	12	16	mA	V_{IN+} = V_{CC1}=5.5 V V_{IN-} = 0V	8, 34, 35	-
Low Level Input Supply Current	I_{CCIL}	-	2.2	3		V_{IN+} = V_{IN-} = 0V, V_{CC1} = 5.5V		-
Output Supply Current	I_{CC2}	-	2.5	5		V_{OUT}= open	9, 10, 36, 37	7
Low Level Collector Current	I_{CL}	-	0.3	1.0		I_{OUT} = 0	13, 56	22
High Level Collector Current	I_{CH}	-	0.3	1.3		I_{OUT} = 0	13, 55	22
		-	1.8	3.0		I_{OUT} = -650 μA	13, 54	
VE Low Level Supply Current	I_{EL}	-0.7	-0.4	0		-	12, 58	-
VE High Level Supply Current	I_{EH}	-0.5	-0.14	0		-	12, 37	20
Blanking Capacitor Charging Current	I_{CHG}	-0.13	-0.24	-0.33		V_{DESAT} =0 - 6V, V_{DESAT} =0 - 6V, T_a = 25°C - 100°C	11, 38	7
Blanking Capacitor Discharge Current	I_{DSCHG}	10	30	-		V_{DESAT} = 7 V	39	-
UVLO Threshold	V_{UVLO+}	11.6	12.3	13.5	V	I_F=10mA,V_{OUT}>5 V	40	5, 7, 8
	V_{UVLO-}	9.2	11.1	12.4		I_F=10mA,V_{OUT}<5 V		5, 7, 9
UVLO Hysteresis	V_{UVLO+} - V_{UVLO-}	-	1.2	-		-		-
DESAT Threshold	V_{DESAT}	6.0	6.7	7.5		V_{CC2} - V_E > V_{UVLO-}	14, 41	7
Threshold input current Low to high	$I_{F(ON)}$	-	2.0	5.0	mA	I_{OUT}=0mA, V_{OUT}>5.0V	-	-
Threshold input voltage High to low	$V_{F(OFF)}$	0.8	-	-	V	I_{OUT}=0mA, V_{OUT}<5.0V	-	-

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Switching Specifications (AC)

Unless otherwise noted, all typical values at T_a= 40°C to 110°C, V_{CC1} = 5V, and V_{CC2} - V_{EE} = 30V, V_E - V_{EE} = 0V; All Minimum/Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig	Note
VIN to High Level Output Propagation Delay Time	t_{PLH}	0.10	0.30	0.50	μs	R_g = 10Ω, C_g = 10nF, f = 10kHz, Duty Cycle = 50%	15, 16, 17, 18, 19, 20, 42, 51, 52	10
VIN to Low Level Output Propagation Delay Time	t_{PHL}	0.10	0..32	0.50				
Pulse Width Distortion	PWD	-80	20	80	ns		-	11, 12
Propagation Delay Difference Between Any Two Parts	PDD	-100	-	100			-	12, 13
10% to 90% Rise Time	t_r	-	50	-			42	-
90% to 10% Fall Time	t_f	-	50	-				-
DESAT Sense to 90% VOUT Delay	$t_{DESAT(90\%)}$	-	0.3	0.5	μs	R_g = 10Ω, C_g = 10nF	21, 53	14
DESAT Sense to 10% VOUT Delay	$t_{DESAT(10\%)}$	-	2.0	3.0		V_{CC2} - V_{EE} =30V	22, 26, 43, 53	-
DESAT Sense to Low Level FAULT Signal Delay	$t_{DESAT(FAULT)}$	-	1.8	5		-	23, 44, 53	15
DESAT Sense to DESAT Low Propagation Delay	$t_{DESAT(LOW)}$	0.1	0.25	1.0		-	53	16
$\overline{\text{RESET}}$ to High Level $\overline{\text{FAULT}}$ Signal Delay	$t_{RESET(FAULT)}$	3	7	20		-	24, 25, 53	17
$\overline{\text{RESET}}$ Signal Pulse Width	$PW_{\overline{RESET}}$	0.1	-	-		-	-	-
UVLO to VOUT High Delay	$t_{UVLO\ ON}$	-	5.0	-		V_{CC2} = 1.0ms ramp	46	8
UVLO to VOUT Low Delay	$t_{UVLO\ OFF}$	-	5.0	-				9
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	15	30	-	kV/μs	T_a=25°C, V_{CM}=1500V, V_{CC2}=30V	47, 48, 49, 50	18
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	15	30	-		T_a=25°C, V_{CM}=1500V, V_{CC2}=30V		19

Notes:

1.In order to achieve the absolute maximum power dissipation specified, pins 4, 9, and 10 require ground plane connections and may require airflow. In most cases the absolute maximum output IC junction temperature is the limiting factor. The actual power dissipation achievable will depend on the application

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environment (PCB Layout, air flow, part placement, etc.). Output IC power dissipation is derated linearly at 10mW/°C above 90°C. Input IC power dissipation does not requirederating.
2.Maximum pulse width =10μs, maximum duty cycle =0.2%. This value is intended to allow for component tolerances for designs with IO peak minimum =2.0A.
3.This supply is optional. Required only when negative gate drive is implemented.
4.Maximum pulse width =50μs, maximum duty cycle =0.5%.
5.15V is the recommended minimum operating positive supply voltage (V_{CC2} - V_E) to ensure adequate margin in excess of the maximum V_U- V_{LO+} threshold of 13.5V. For High Level Output Voltage testing, V_{OH} is measured with a dc load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zerounits.
6.Maximum pulse width = 1.0ms, maximum duty cycle = 20%.
7.Once V_{OUT} of the ICPL-316J is allowed to go high (V_{CC2}-V_E>V_{UVLO}), the DESAT detection feature of the ICPL-316J will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once V_{UVLO+}>11.6V, DESAT will remain functional until V_{UVLO-} <12.4V. Thus, the DESAT detection and UVLO features of the ICPL-316J work in conjunction to ensure constant IGBT protection.
8.This is the “increasing”(i.e. turn-on or “positive going” direction) of V_{CC2}-V_E.
9.This is the “decreasing”(i.e. turn-off or “negative going” direction) of V_{CC2}-V_E.
10.This load condition approximates the gate load of a 1200 V/75A IGBT.
11.Pulse Width Distortion (PWD) is defined as |t_{PHL}- t_{PLH}| for any given unit.
12.As measured from V_{IN+}, V_{IN-} to V_{OUT}.
13.The difference between t_{PHL} and t_{PLH} between any two ICPL-316J parts under the same test conditions.
14.Supply Voltage Dependent.
15.This is the amount of time from when the DESAT threshold is exceeded, until the FAULT output goes low.
16.This is the amount of time the DESAT threshold must be exceeded before V_{OUT} begins to go low, and the FAULT output to go low.
17.This is the amount of time from when RESET is asserted low, until FAUL Toutput goes high. The minimum specification of 3 μs is the guaran- teed minimum FAULT signal pulse width when the ICPL-316J is configured for Auto-Reset.
18.Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O >15V or FAULT>2V). A 100 pF and a 3KΩ pull-up resistor is needed in fault detection mode.
19.Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O<1.0V or FAULT<0.8V).
20.Does not include LED2 current during fault or blanking capacitor discharge current.
21.To clamp the output voltage at V_{CC} - $3V_{BE}$, a pull-down resistor between the output and V_{EE} is recommended to sink a static current of 650μA while the output is high.
22.The recommended output pull-down resistor between V_{OUT} and V_{EE} does not contribute any output current when V_{OUT} = V_{EE}.
23.In most applications V_{CC1} will be powered up first (before V_{CC2}) and powered down last (after V_{CC2}). This is desirable for maintaining control of the IGBT gate. In applications where V_{CC2} is powered up first, it is important to ensure that V_{in+} remains low until V_{CC1} reaches the proper operating voltage (minimum 4.5V) to avoid any momentary instability at the output during V_{CC1} ramp-up or ramp-down.

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TYPICAL PERFORMANCE CURVES

Fig.1 I_{OH} vs. Temperature.

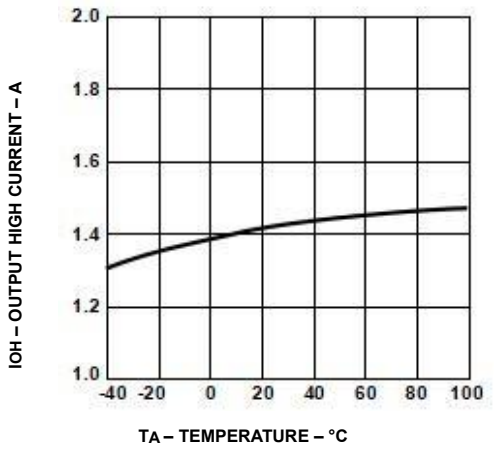

Fig.2 V_{OH} vs. Temperature

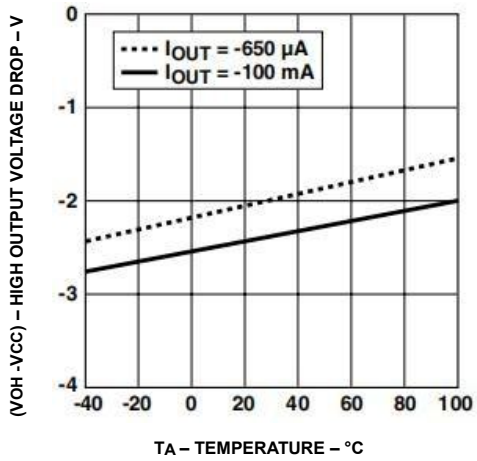

Fig.3 V_{OL} vs. Temperature

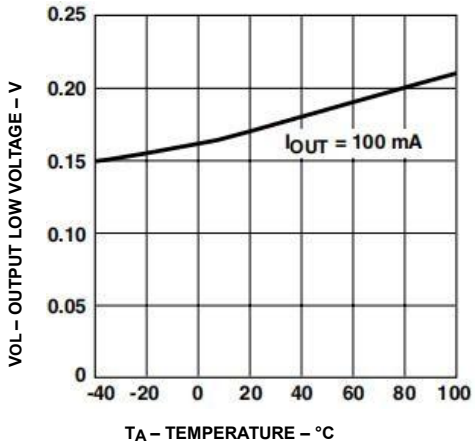

Fig.4 V_{OH} vs. I_{OH}

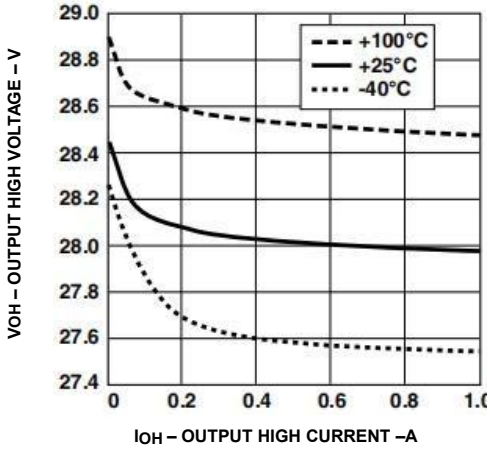

Fig.5 V_{OL} vs. I_{OL}

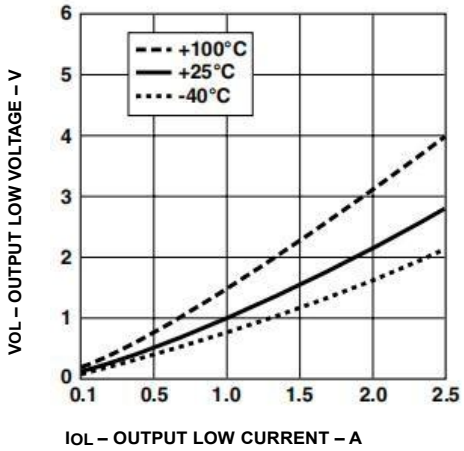

Fig. 6 I_{CC2} vs. Temperature

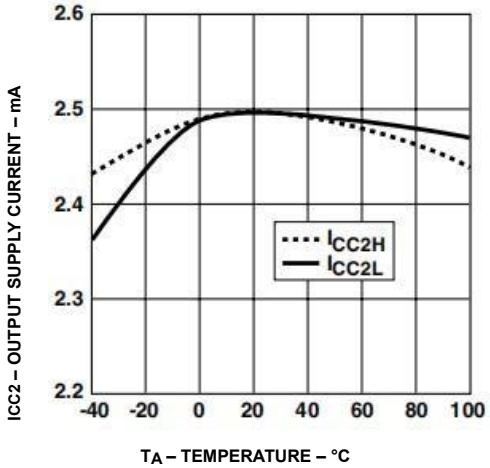

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Fig.7 I_{CC2} vs. V_{CC2}

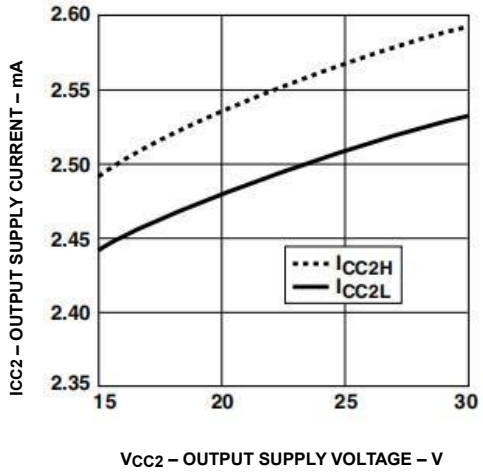

Fig.8 I_{CHG} vs. Temperature

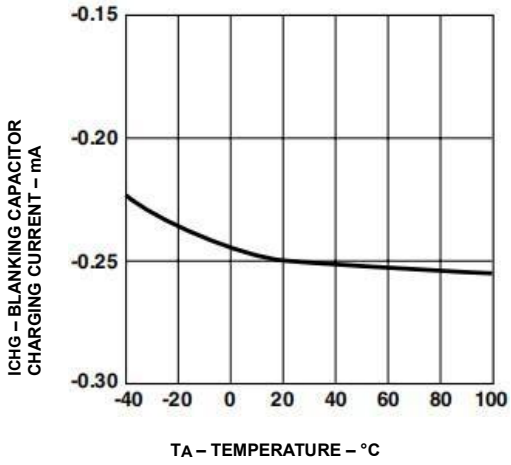

Fig.9 DESAT threshold vs. Temperature

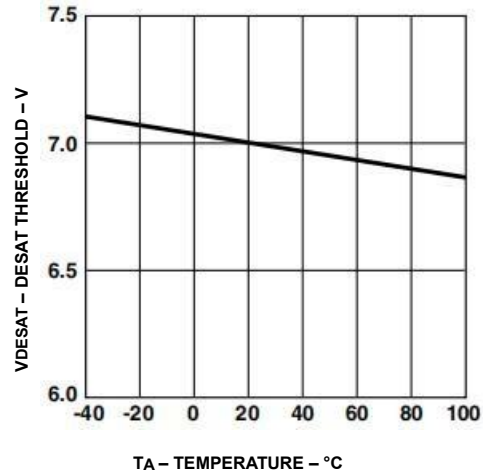

Fig.10 Propagation delay vs. Temperature

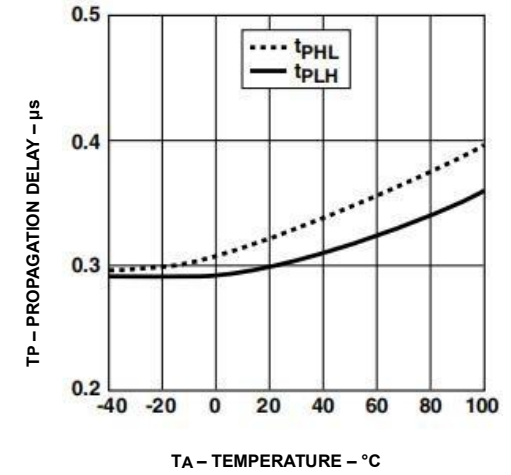

Fig.11 Propagation delay vs. supply voltage

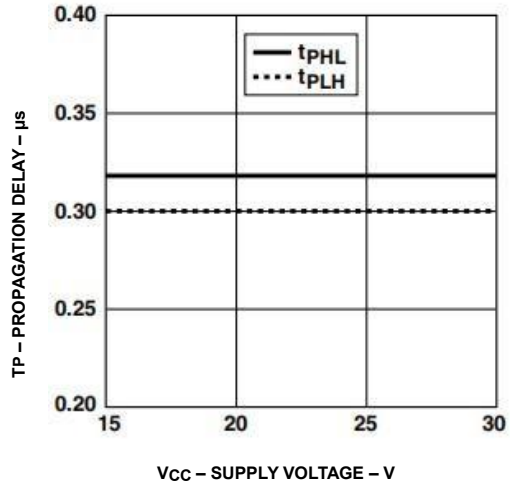

Fig.12 Propagation delay vs. load resistance

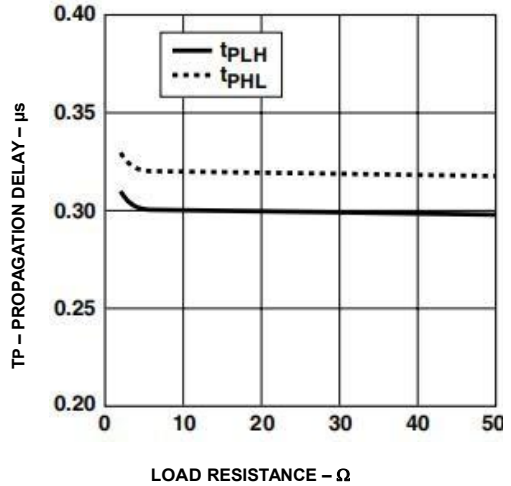

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Fig.13 Propagation delay vs. load capacitance

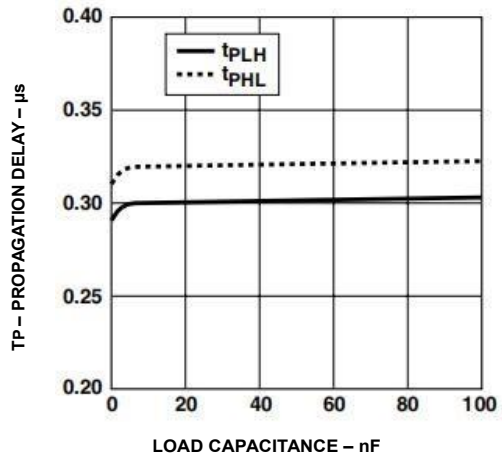

Fig.14 DESAT sense to 90% V_{OUT} delay vs. temperature

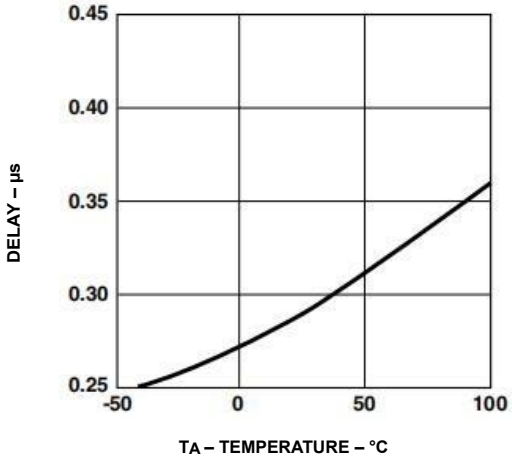

Fig.15 DESAT sense to 10% V_{OUT} delay vs. temperature

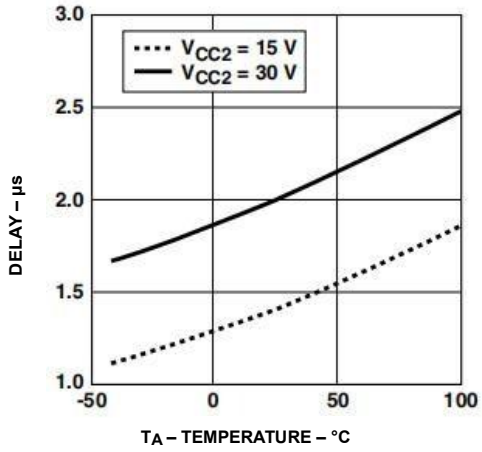

Fig.16 DESAT sense to 10% V_{OUT} delay vs. load resistance

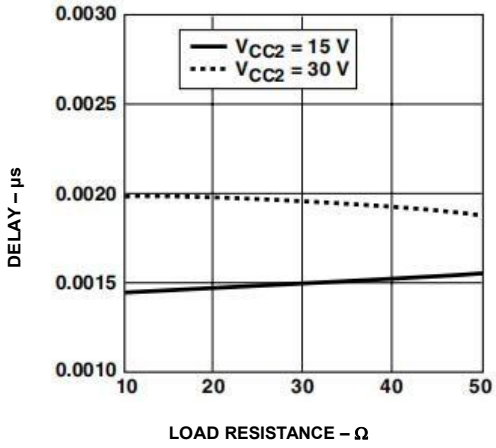

Fig.17 DESAT sense to 10% V_{OUT} delay vs. load capacitance

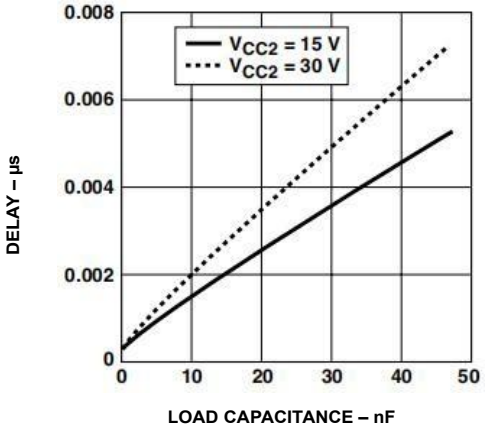

Fig.18 DESAT sense to low level fault signal delay vs. temperature

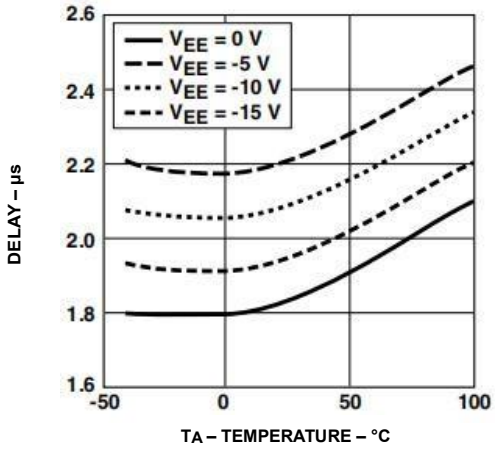

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Fig.19 RESET to high level fault signal delay vs. temperature

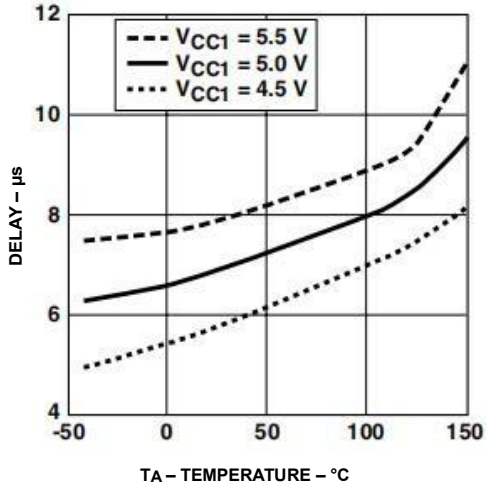

Fig.20 I_C vs. I_{OUT}

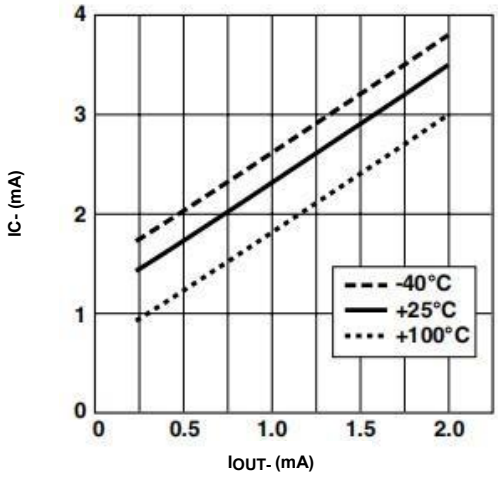

Fig.21 I_{OL} vs. Temperature

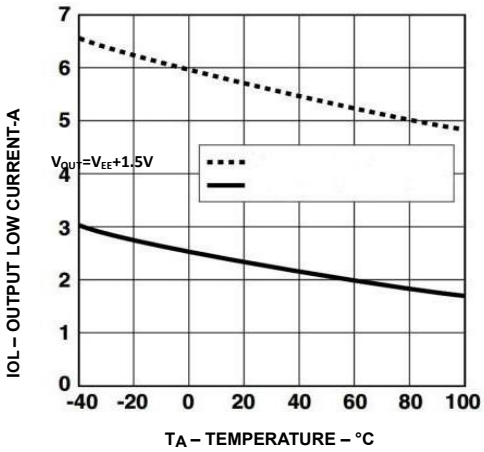

Fig.22 I_{OLF} vs. V_{OUT}

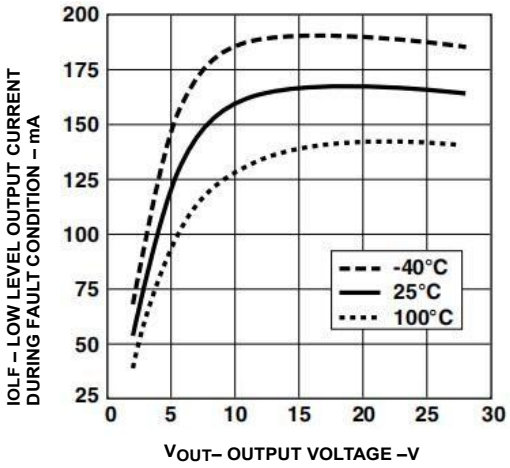

Fig.23 I_{CC1} vs. Temperature.

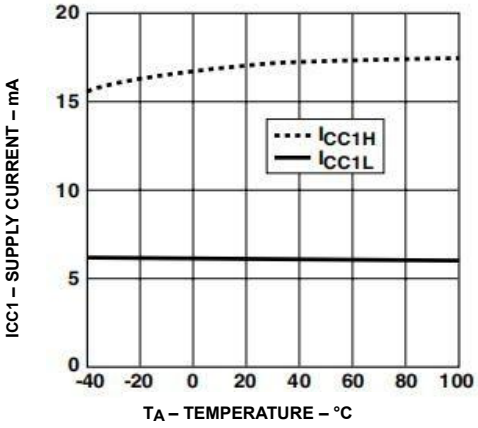

Fig.24 I_E vs. Temperature.

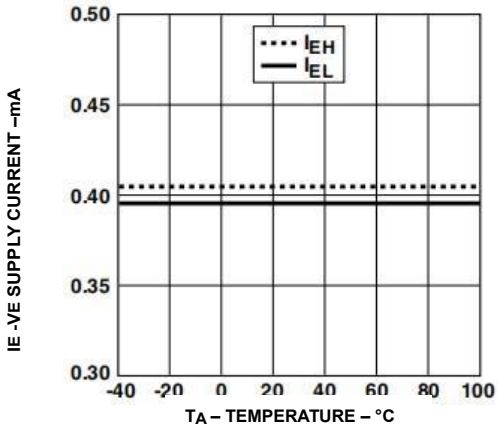

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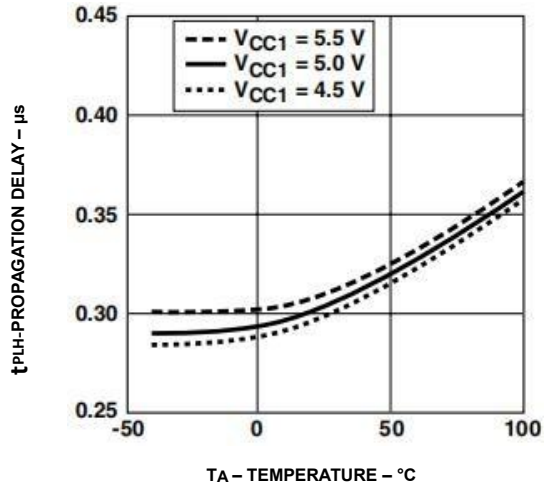
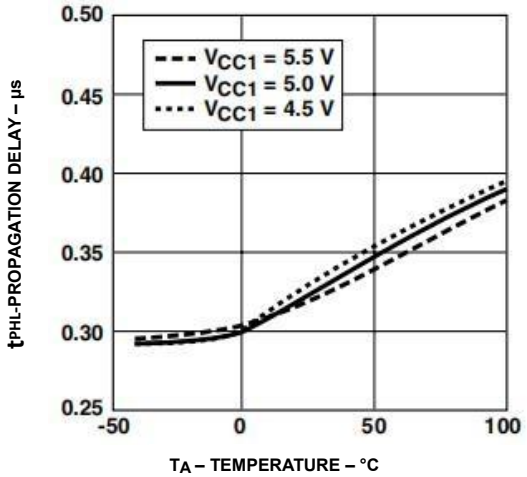
Fig.25 V_{IN} to high propagation delay vs. Temperature	Fig.26 V_{IN} to low propagation delay vs. Temperature.
	

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TEST CIRCUITS

Fig.27 I_{OH} Pulsed test circuit

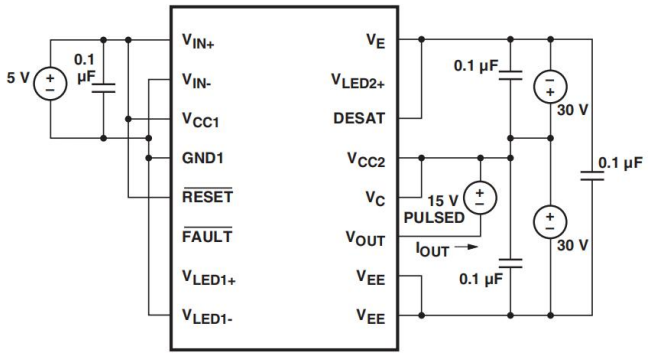

Fig.28 I_{OL} Pulsed test circuit

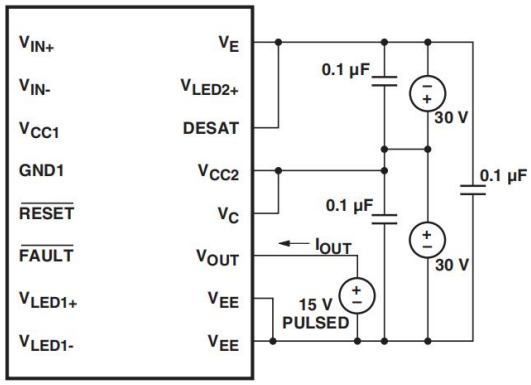

Fig.29 V_{OH} Pulsed test circuit

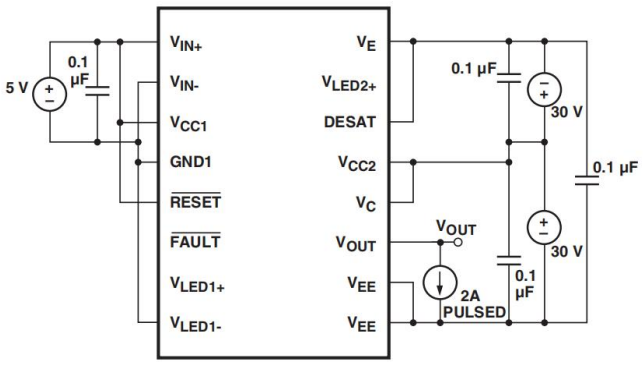

Fig.30 V_{OL} Pulsed test circuit

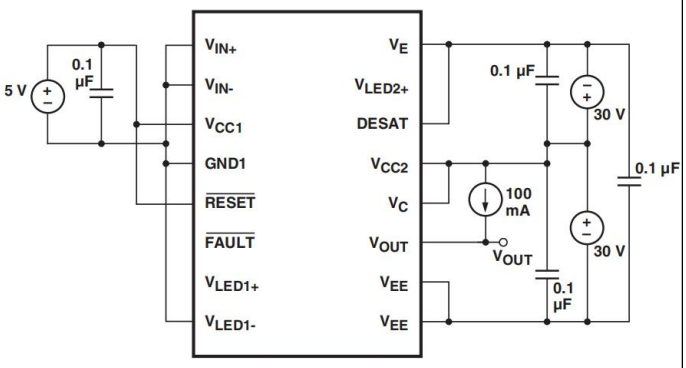

Fig.31 I_{CC2H} test circuit

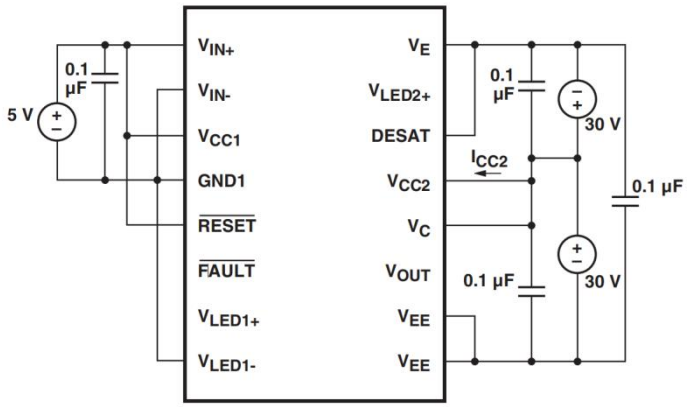

Fig.32 I_{CC2L} test circuit

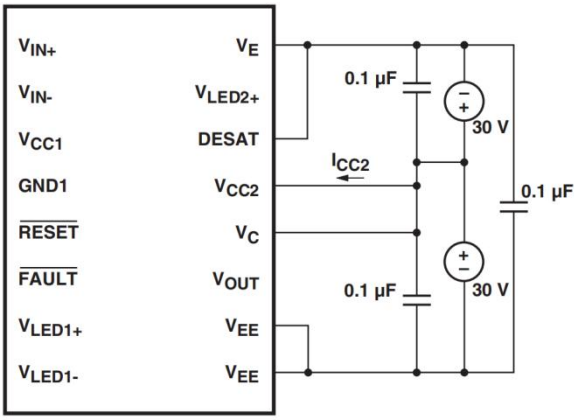

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Fig.33 I_{CHG} Pulsed test circuit

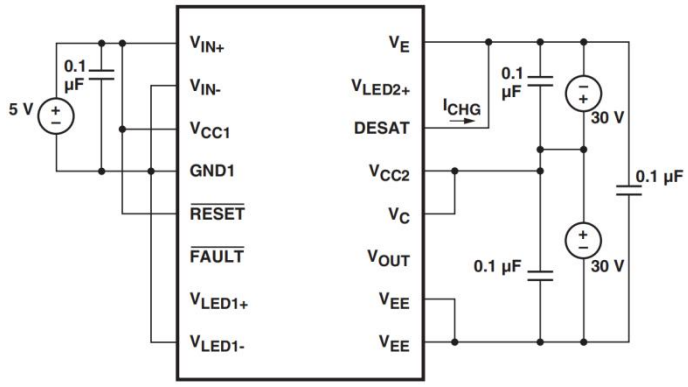

Fig.34 I_{DSCHG} test circuit

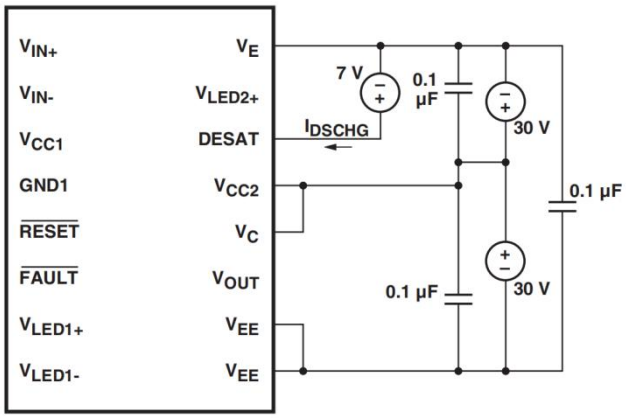

Fig.35 t_{PLH}, t_{PHL}, t_f, t_r, test circuit

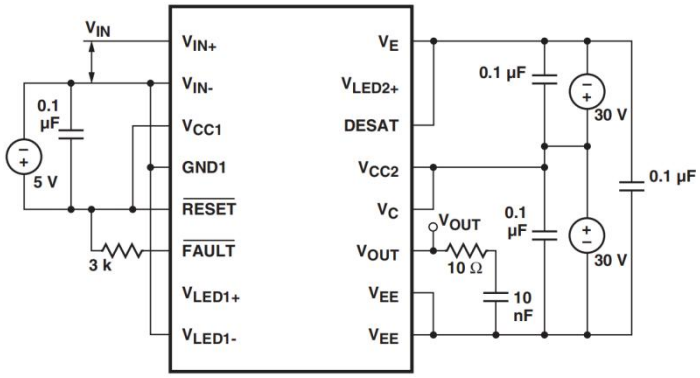

Fig.36 t_{DESAT} fault test circuit

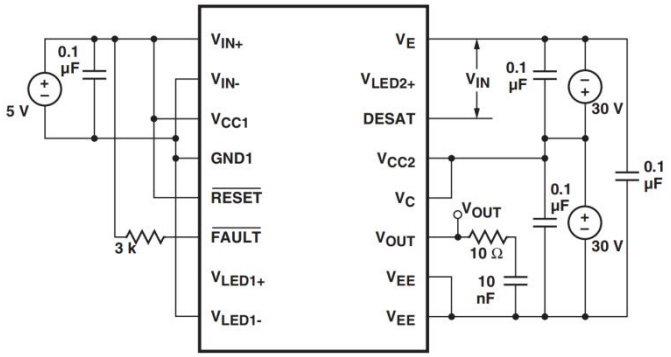

Fig.37 CMR Test circuit LED2 off

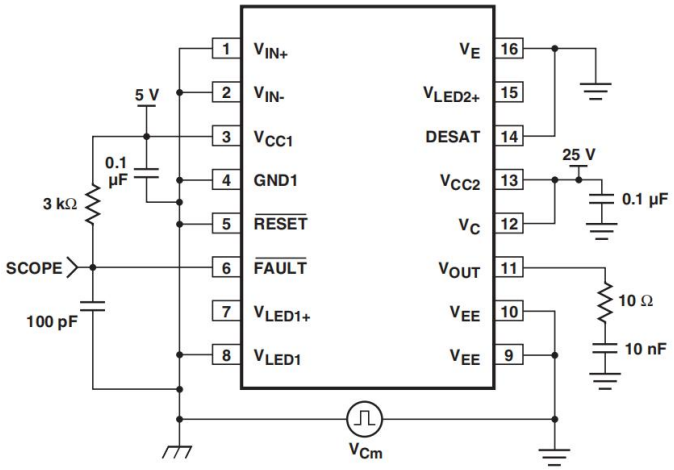

Fig.38 CMR Test Circuit LED2 on

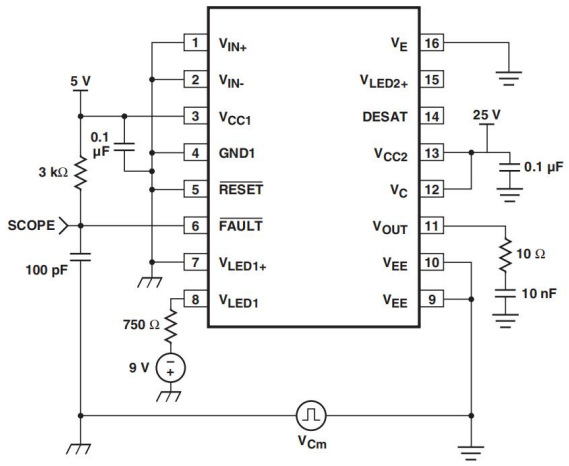

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Fig.39 CMR Test circuit LED1 off

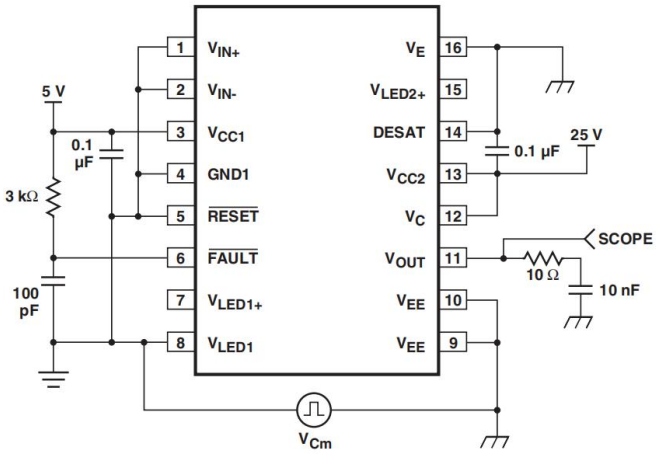

Fig.40 CMR Test Circuit LED1 on

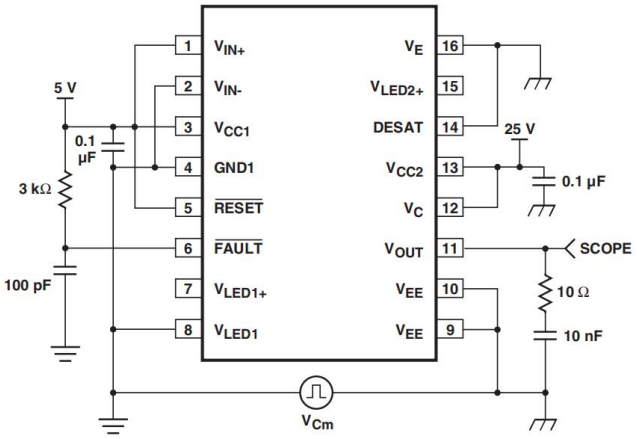

Fig.41 I_{FAULTL} Test Circuit

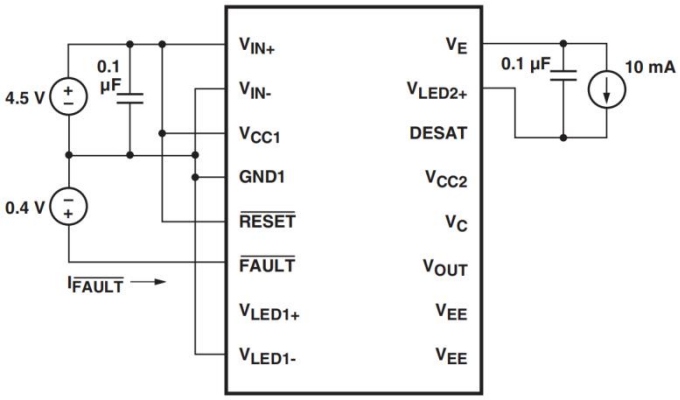

Fig.42 I_{FAULTH} Test Circuit

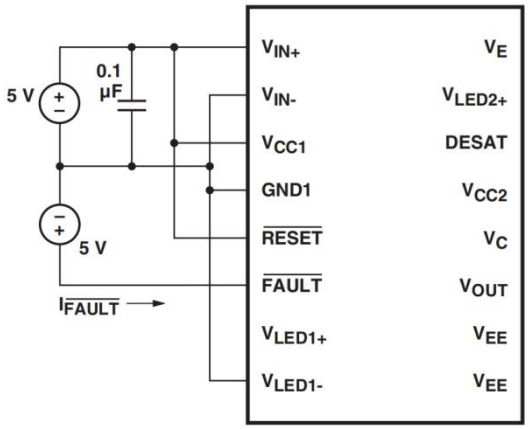

Fig.43 I_{OLF} Test Circuit

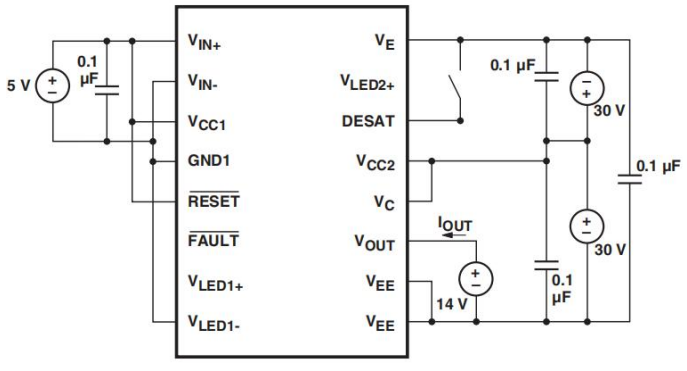

Fig.44 I_{CC1H} test circuit

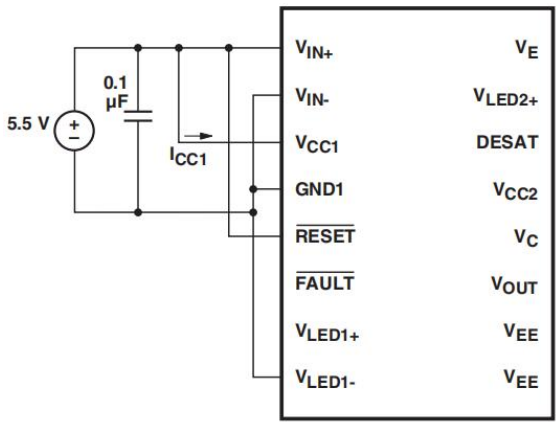

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Fig.45 I_{CC1L} test circuit

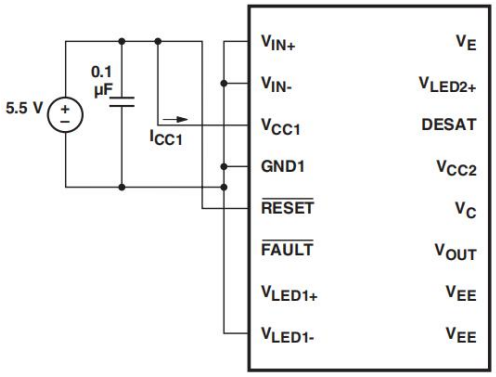

Fig.46 UVLO threshold test circuit

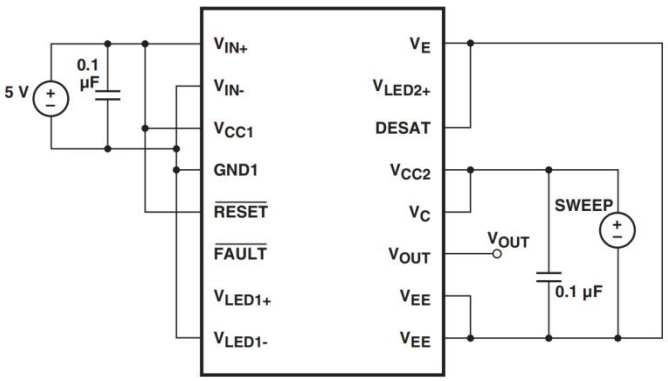

Fig.47 DESAT threshold test circuit.

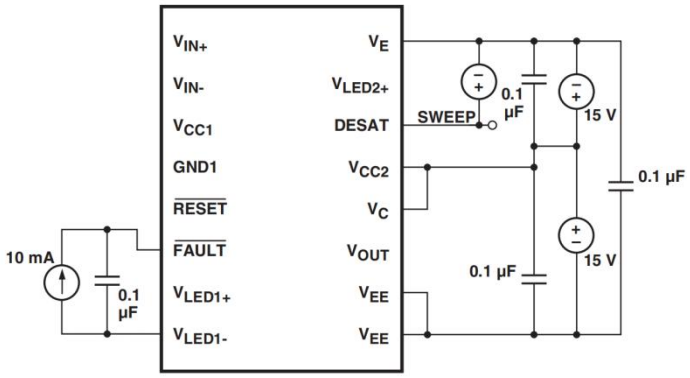

Fig.48 $t_{DESAT(10\%)}$ test circuit

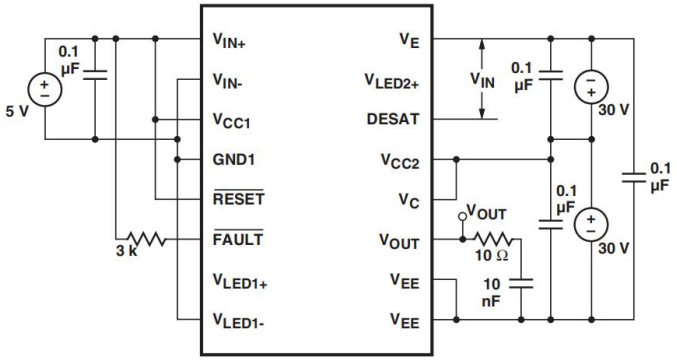

Fig.49 $t_{RESET(FAULT)}$ test circuit .

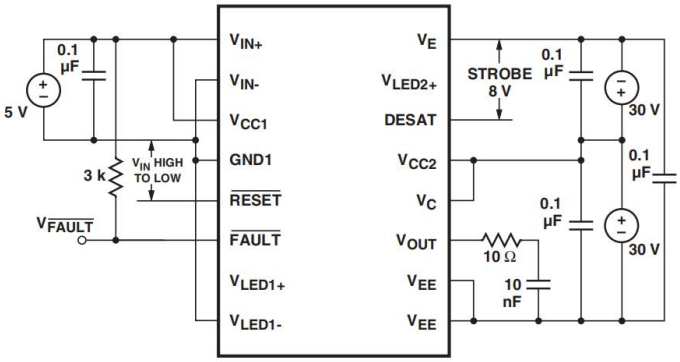

Fig.50 UVLO delay test circuit.

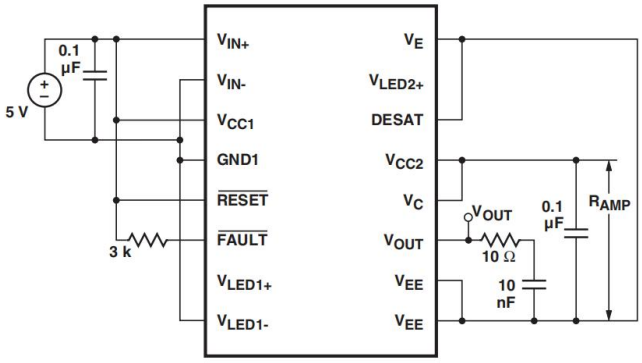

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Fig.51 V_{OUT} propagation delay waveforms, noninverting configuration.

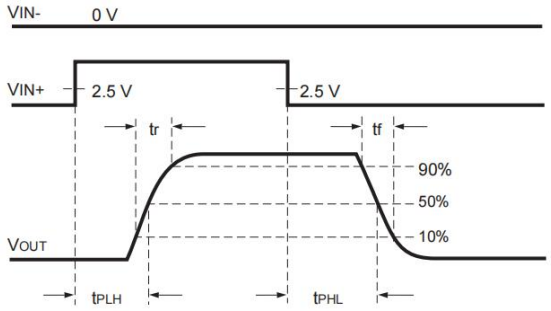

Fig.52 V_{OUT} propagation delay waveforms, inverting configuration.

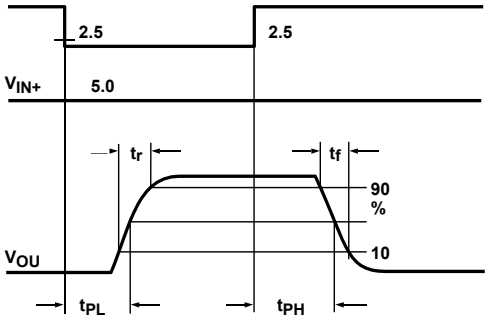

Fig.53 Desat, V_{OUT}, fault, reset delay waveforms.

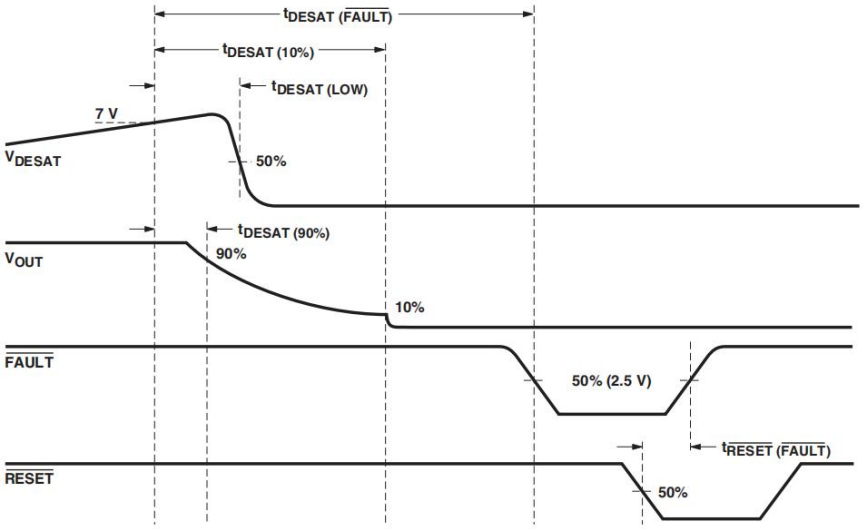

Fig.54 I_{CH} test circuit

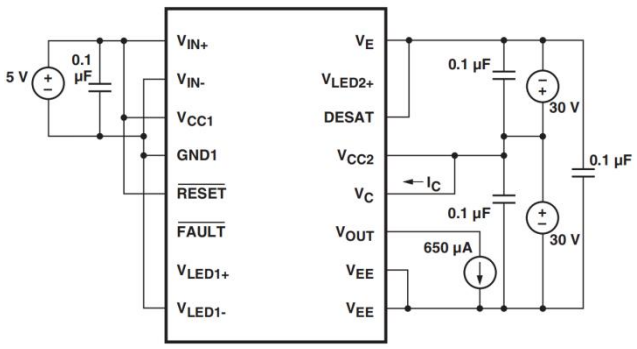

Fig.55 I_{CH} test circuit

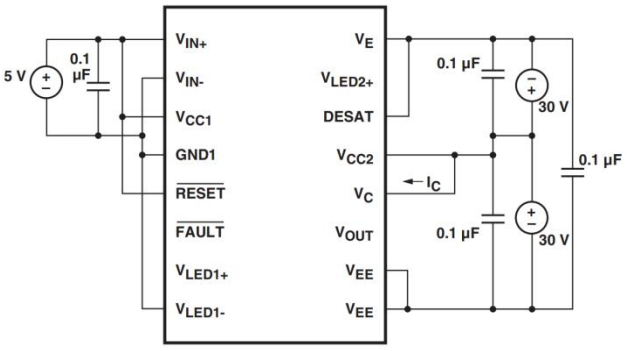

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Fig.56 I_{CL} test circuit

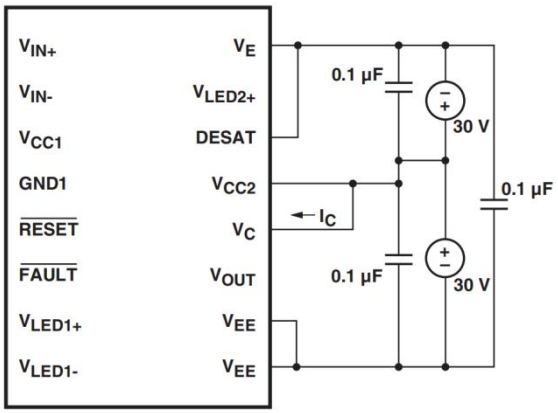


Fig.57 I_{EH} test circuit

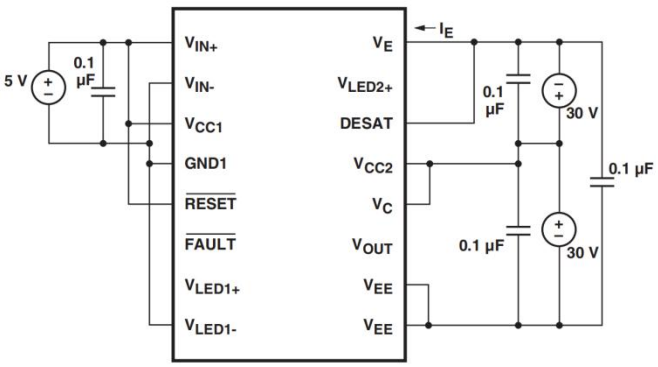
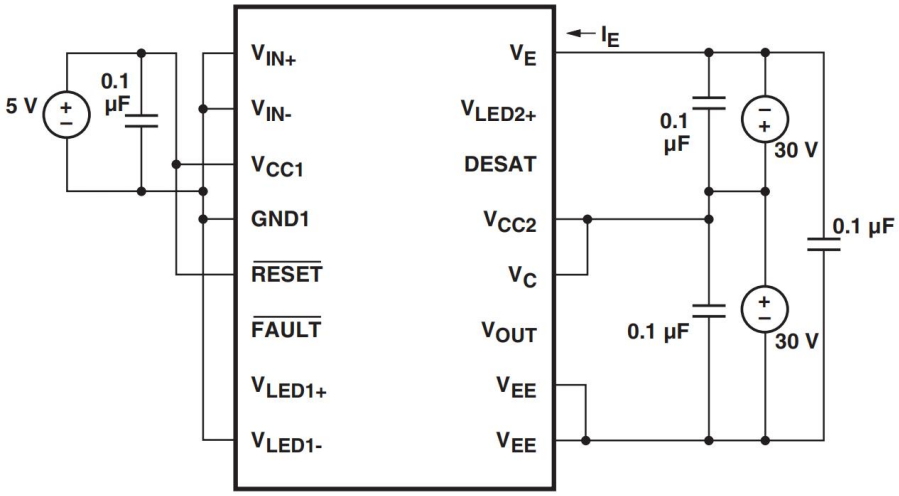


Fig.58 I_{EL} test circuit



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Typical Application/Operation

Introduction to Fault Detection and Protection

The power stage of a typical three phase inverter is susceptible to several types of failures, most of which are potentially destructive to the power IGBTs. These failure modes can be grouped into four basic categories: phase and/or rail supply short circuits due to user misconnect or bad wiring, control signal failures due to noise or computational errors, overload conditions induced by the load, and component failures in the gate drive circuitry. Under any of these fault conditions, the current through the IGBTs can increase rapidly, causing excessive power dissipation and heating. The IGBTs become damaged when the current load approaches the saturation current of the device, and the collector to emitter voltage rises above the saturation voltage level. The drastically increased power dissipation very quickly overheats the power device and destroys it. To prevent damage to the drive, fault protection must be implemented to reduce or turn-off the over currents during a fault condition.

A circuit providing fast local fault detection and shut-down is an ideal solution, but the number of required components, board space consumed, cost, and complexity have until now limited its use to high performance drives. The features which this circuit must have are high speed, low cost, low resolution, low power dissipation, and small size.

Applications Information

The ICPL-316J satisfies these criteria by combining a high speed, high output current driver, high voltage optical isolation between the input and output, local IGBT desaturation detection and shut down, and an optically isolated fault status feedback signal into a single 16-pin surface mount package.

The fault detection method, which is adopted in the ICPL-316J, is to monitor the saturation (collector) voltage of the IGBT and to trigger a local fault shutdown sequence if the collector voltage exceeds a predetermined threshold. A small gate discharge device slowly reduces the high short circuit IGBT current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is shut off. During the off state of the IGBT, the fault detect circuitry is simply disabled to prevent false ‘fault’ signals.

The alternative protection scheme of measuring IGBT current to prevent desaturation is effective if the short circuit capability of the power device is known, but this method will fail if the gate drive voltage decreases enough to only partially turn on the IGBT. By directly measuring the collector voltage, the ICPL-316J limits the power dissipation in the IGBT even with insufficient gate drive voltage. Another more subtle advantage of the desaturation detection method is that power dissipation in the IGBT is monitored, while the current sense method relies on a preset current threshold to predict the safe limit of operation. Therefore, an overly-conservative overcurrent threshold is not needed to protect the IGBT.

Recommended Application Circuit

The ICPL-316J has both inverting and non-inverting gate control inputs, an active low reset input, and an open collector fault output suitable for wired ‘OR’ applications. The recommended application circuit shown in Figure 59 illustrates a typical gate drive implementation using the ICPL-316J.

The four supply bypass capacitors (0.1 μF) provide the large transient currents necessary during a switching transition.

Because of the transient nature of the charging currents, a low current (5 mA) power supply suffices. The desat diode and 100 pF capacitor are the necessary external components for the fault detection circuitry. The gate resistor (10 Ω) serves to limit gate charge current and indirectly control the IGBT collector voltage rise and fall times. The open collector fault output has a passive 3.3 kΩ pull-up resistor and a 330 pF filtering capacitor. A 47 kΩ pulldown resistor on V_{OUT} provides a more predictable high level output voltage (V_{OH}). In this application, the IGBT gate driver will shut down when a fault is detected and will not resume switching until the microcontroller applies a reset signal.

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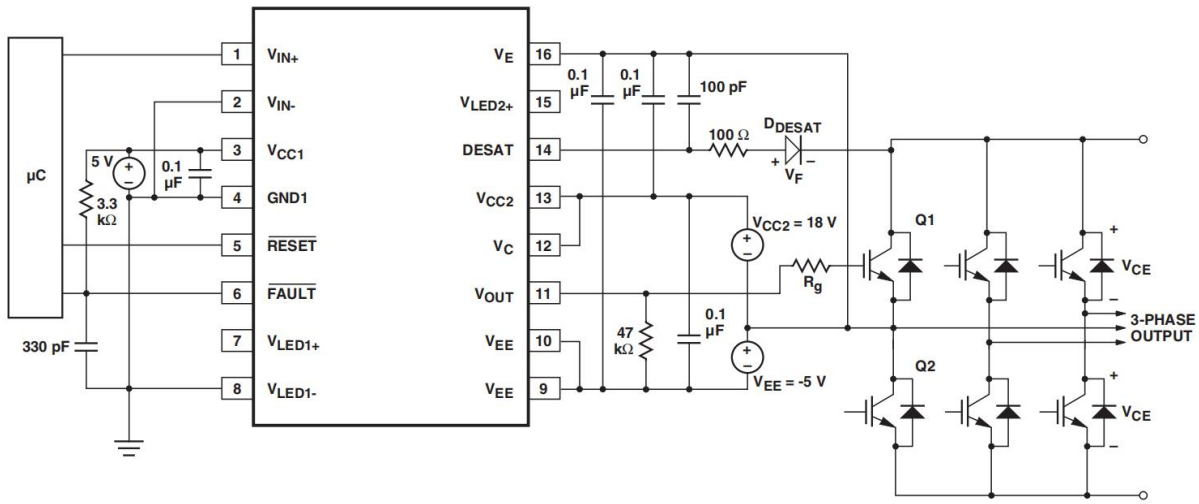
Fig 59. Recommended application circuit.



Behavioral Circuit Schematic

The function albehavior of the ICPL-316J is represented by thelogic diagram in Figure 60 which fully describesthe interactionandsequenceof internalandexternalsignals inthe ICPL-316J.

Input IC

In the normal switching mode, no output fault has been detected, and the low state of the fault latch allows the input signals to control the signal LED. The faultoutput is in the open-collector state, and the state of the Reset pin does not affect the control of the IGBT gate. When a fault is detected, the FAULT output and signal inputare both latched. The fault output changes to an active low state, and the signal LED is forced off (output LOW). The latched condition will persist until the Reset pin is pulled low.

Output IC

Three internal signals control the state of the driver output: the state of the signal LED, as well as the UVLO and Fault signals. If no fault on the IGBT collector is detected, and the supply voltage is above the UVLO threshold, the LED signal will control the driver output state. The driver stage logic includes an interlock to ensure that the pull-up and pull-down devices in the output stage are never on at the same time. If an undervoltage condition is detected, the output will be actively pulled low by the 50x DMOS device, regardless of the LED state. If an IGBT desaturation fault is detected while the signal LED is on, the Fault signal will latch in the high state. The triple dar- lington AND the 50x DMOS device are disabled, and a smaller 1x DMOS pull-down device is activated to slowly discharge the IGBT gate. When the output drops below two volts, the 50x DMOS device again turns on, clamping the IGBT gate firmly to VEE. The Fault signal remains latched in the high state until the signal LED turns off.

Figure 60. Behavioral Circuit Schematic

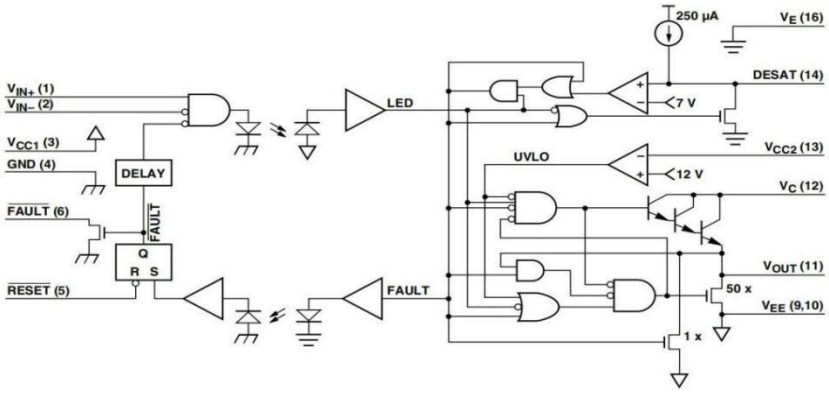


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Fig.61 Output pull-down resistor

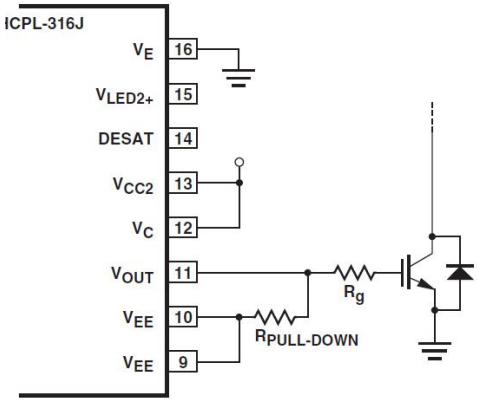


Fig.62 DESAT pin protection

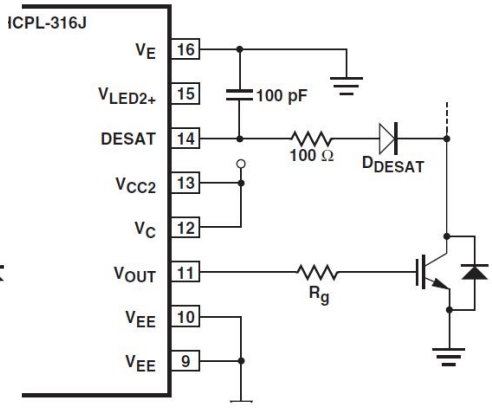
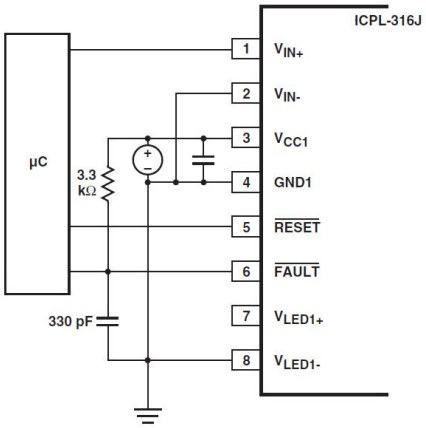


Fig.63 FAULT pin CMR protection



Other Recommended Components

The application circuit in Figure 59 includes an output pull-down resistor, a DESAT pin protection resistor, a FAULT pin capacitor (330 pF), and a FAULT pin pull-up resistor.

Output Pull-Down Resistor

During the output high transition, the output voltage rapidly rises to within 3 diode drops of V_{CC2}. If the output current then drops to zero due to a capacitive load, the output voltage will slowly rise from roughly V_{CC2}-3(V_{BE}) to V_{CC2} within a period of several microseconds. To limit the output voltage to V_{CC2}-3(V_{BE}), a pull-down resistor between the output and V_{EE} is recommended to sink a static current of several 650 μA while the output is high. Pull-down resistor values are dependent on the amount of positive supply and can be adjusted according to the formula, Rpull-down = [V_{CC2}-3 * (V_{BE})] / 650 μA.

DESAT Pin Protection

The freewheeling of flyback diodes connected across the IGBTs can have large instantaneous forward voltage transients which greatly exceed the nominal forward voltage of the diode. This may result in a large negative voltage spike on the DESAT pin which will draw substantial current out of the IC if protection is not used. To limit this current to levels that will not damage the IC, a 100 ohm resistor should be inserted in series with the DESAT diode. The added resistance will not alter the DESAT threshold or the DESAT blanking time.

Capacitor on FAULT Pin for High CMR

Rapid common mode transients can affect the fault pin voltage while the fault output is in the high state. A 330 pF capacitor (Fig. 62) should be connected between the fault pin and ground to achieve adequate CMOS noise margins at the specified CMR value of 15 kV/μs. The added capacitance does not increase the fault output delay when a desaturation condition is detected.

Pull-up Resistor on FAULT Pin

The FAULT pin is an open-collector output and therefore requires a pull-up resistor to provide a high-level signal.

Driving with Standard CMOS/TTL for High CMR

Capacitive coupling from the isolated high voltage circuitry to the input referred circuitry is the primary CMR limitation. This coupling must be accounted for to achieve high CMR performance. The input pins V_{IN+} and V_{IN-} must have active drive signals to prevent unwanted switching of the output under extreme common mode transient conditions. Input drive circuits that use pull-up or pull-down resistors, such as open collector configurations, should be avoided. Standard CMOS or TTL drive circuits are recommended.

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User-Configuration of the ICPL-316J Input Side

The V_{IN+}, V_{IN-}, FAULT and RESET input pins make a wide variety of gate control and fault configurations possible, depending on the motor drive requirements. The ICPL-316J has both inverting and noninverting gate control inputs, an open collector fault output suitable for wired 'OR' applications and an active low reset input.

Driving Input pf ICPL-316J in Non-Inverting/Inverting Mode

The Gate Drive Voltage Output of the ICPL-316J can be configured as inverting or non-inverting using the V_{IN-} and V_{IN+} inputs. As shown in Figure 64, when a non-inverting configuration is desired, V_{IN-} is held low by connecting it to GND1 and V_{IN+} is toggled. As shown in Figure 65, when an inverting configuration is desired, V_{IN+} is held high by connecting it to VCC1 and V_{IN-} is toggled.

Local Shutdown, Local Reset

As shown in Figure 66, the fault output of each ICPL-316J gate driver is polled separately, and the individual reset lines are asserted low independently to reset the motor controller after a fault condition.

Global-Shutdown, Global Reset

As shown in Figure 67, when configured for inverting operation, the ICPL-316J can be configured to shutdown automatically in the event of a fault condition by tying the FAULT output to V_{IN+}. For high reliability drives, the open collector FAULT outputs of each ICPL-316J can be wire 'OR'ed together on a common fault bus, forming a single fault bus for interfacing directly to the micro-controller. When any of the six gate drivers detects a fault, the fault output signal will disable all six ICPL-316J gate drivers simultaneously and thereby provide protection against further catastrophic failures.

Fig.64 Typical input configuration, noninverting.

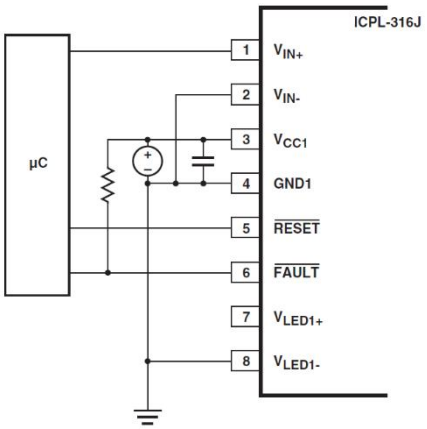


Fig.65 Typical Input Configuration, Inverting.

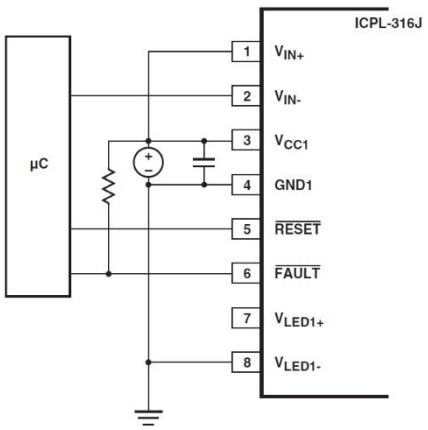
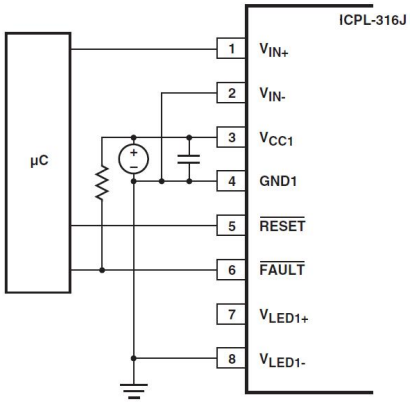


Fig.66 Local shutdown, local reset configuration.



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Auto-Reset

As shown in Figure 68, when the inverting V_{IN-} input is connected to ground (non-inverting configuration), the ICPL-316J can be configured to reset automatically by connecting RESET to V_{IN+}. In this case, the gate control signal is applied to the non-inverting input as well as the reset input to reset the fault latch every switching cycle. During normal operation of the IGBT, asserting the reset input low has no effect. Following a fault condition, the gate driver remains in the latched fault state until the gate control signal changes to the 'gate low' state and resets the fault latch. If the gate control signal is a continuous PWM signal, the fault latch will always be reset by the next time the input signal goes high. This configuration protects the IGBT on a cycle-by-cycle basis and automatically resets before the next 'on' cycle. The fault outputs can be wire 'OR'ed together to alert the microcontroller, but this signal would not be used for control purposes in this (Auto-Reset) configuration. When the ICPL-316J is configured for Auto-Reset, the guaranteed minimum FAULT signal pulse width is 3 µs.

Resetting Following a Fault Condition

To resume normal switching operation following a fault condition (FAULT output low), the RESET pin must first be asserted low in order to release the internal fault latch and reset the FAULT output (high). Prior to asserting the RESET pin low, the input (V_{IN}) switching signals must be configured for an output (V_{OL}) low state. This can be handled directly by the microcontroller or by hardwiring to synchronize the RESET signal with the appropriate input signal. Figure 69a shows how to connect the RESET to the V_{IN+} signal for safe automatic reset in the noninverting input configuration. Figure 69b shows how to configure the V_{IN+}/RESET signals so that a RESET signal from the microcontroller causes the input to be in the "output-off" state. Similarly, Figures 69c and 69d show automatic RESET and microcontroller RESET safe configurations for the inverting input configuration.

Fig.67 Global-shutdown, global reset configuration

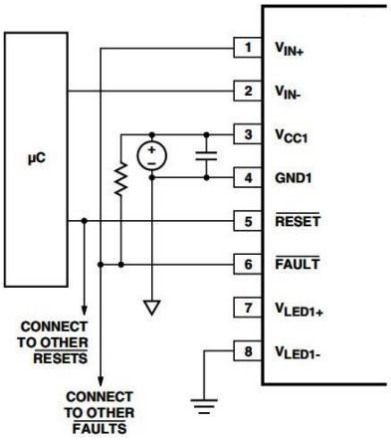


Fig68. Auto-reset configuration

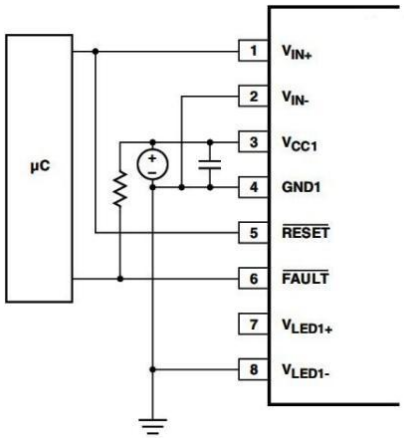


Fig69a. Safe hardware reset for noninverting input configuration (automatically resets for every VIN+ input)

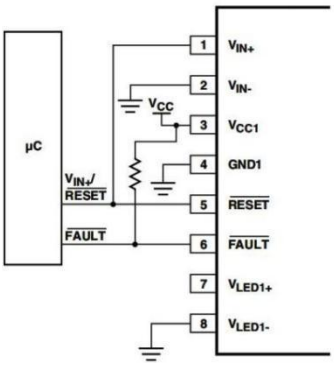
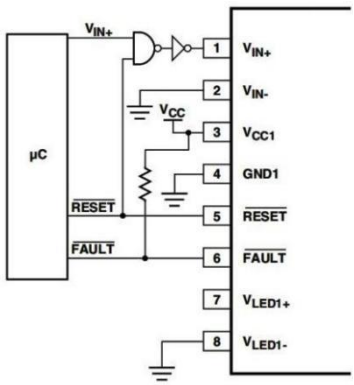


Figure 69b. Safe hardware reset for onfiguration



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User-Configuration of the ICPL-316J Output Side RG and Optional Resistor RC:
The value of the gate resistor RG (along with V_{CC2} and V_{EE}) determines the maximum amount of gate-charging/discharging current (I_{ON},PEAK and I_{OFF},PEAK) and thus should be carefully chosen to match the size of the IGBT being driven. Often it is desirable to have the peak gate charge current be somewhat less than the peak discharge current (I_{ON},PEAK < I_{OFF},PEAK). For this condition, an optional resistor (RC) can be used along with RG to independently determine I_{ON},PEAK and I_{OFF},PEAK without using a steering diode. As an example, refer to Figure 70. Assuming that RG is already determined and that the design I_{OH},PEAK =0.5 A, the value of RC can be estimated in the following way:

$$R_C + R_G = \frac{[V_{CC2} - V_{OH} - (V_{EE})]}{I_{OH,PEAK}}$$

$$= \frac{[4\ V - (-5\ V)]}{0.5\ A}$$

$$= 18\ \Omega$$

$$R_C = 8\ \Omega$$

Fig.69c Safe hardware reset for inverting input configuration

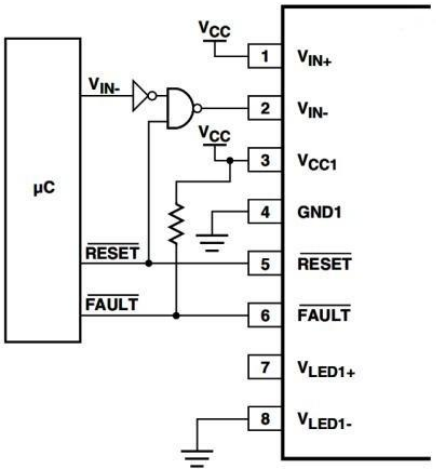


Fig.69d Safe hardware reset for inverting input configuration (automatically resets for every VIN- input)

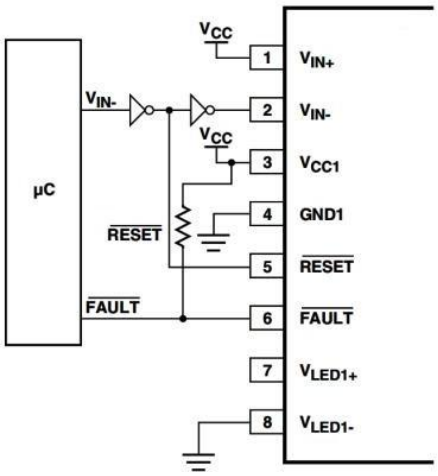


Fig.70 Use of RC to further limit ION, PEAK

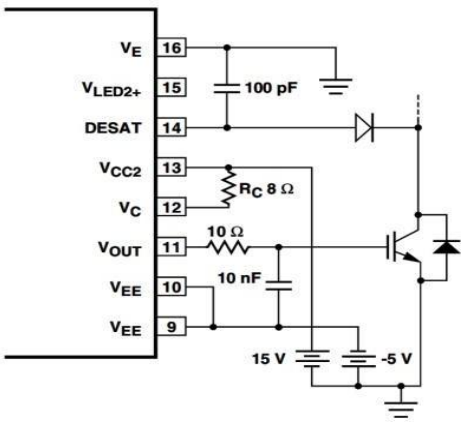
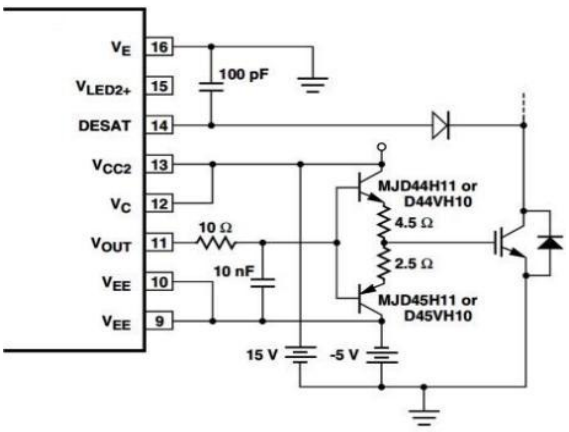


Fig.71 Current buffer for increased drive current



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Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a non-inverting current buffer (such as the npn/pnp buffer shown in Figure 71) may be used. Inverting types are not compatible with the desaturation fault protection circuitry and should be avoided. To preserve the slow IGBT turn-off fea- ture during a fault condition, a 10 nF capacitor should be connected from the buffer input to V_{EE} and a 10 Ω resistor inserted between the output and the common npn/ pnp base. The MJD44H11/MJD45H11 pair is appropriate for currents up to 8A maximum. The D44VH10/ D45VH10 pair is appropriate for currents up to 15 A maximum.

DESAT Diode and DESAT Threshold

The DESAT diode's function is to conduct forward current, allowing sensing of the IGBT's saturated collector-to-emitter voltage, V_{CESAT}, (when the IGBT is "on") and to block high voltages (when the IGBT is "off"). During the short period of time when the IGBT is switching, there is commonly a very high dV_{CE}/dt voltage ramp rate across the IGBT's collector- to-emitter. This results in I_{CHARGE} (= $C_{D\text{-}DESAT}$ x dV_{CE}/dt) charging current which will charge the blanking capacitor, C_{BLANK}. In order to minimize this charging current and avoid false DESAT triggering, it is best to use fast response diodes. In the recommended application circuit shown in Figure 59, the voltage on pin 14 (DESAT) is $V_{DESAT} = V_F + V_{CE}$, (where VF is the forward ON voltage of D_{DESAT} and V_{CE} is the IGBT collector-to-emitter voltage). The value of VCE which triggers DESAT to signal a FAULT condition, is nominally 7V – V_F. If desired, this DESAT threshold voltage can be decreased by using multiple DESAT diodes in series. If *n* is the number of DESAT diodes then the nominal threshold value becomes $V_{CE,FAULT(TH)} = 7\ V - n \times V_F$. In the case of using two diodes instead of one, diodes with half of the total required maximum reverse-voltage rating may be chosen.

Power/Layout Considerations

Operating Within the Maximum Allowable Power Ratings (Adjusting Value of R_G):

When choosing the value of R_G, it is important to confirm that the power dissipation of the ICPL-316J is within the maximum allowable power rating.

The steps for doing this are:

1.Calculate the minimum desired RG;

2.Calculate total power dissipation in the part referring to Figure 73. (Average switching energy supplied to ICPL-316J per cycle vs. RG plot)

3.Compare the input and output power dissipation calculated in step #2 to the maximum recommended dissipation for the ICPL-316J.

(If the maximum recommended level has been exceeded, it may be necessary to raise the value of RG to lower the switching power and repeat step #2.)

As an example, the total input and output power dis- sipation can be calculated given the following conditions:

- I_{ON}, MAX ~ 2.0 A
- V_{CC2} = 18V
- V_{EE} = -5V
- $f_{CARRIER}$ = 15 kHz

Step 1: Calculate R_G minimum from I_{OL} peak specification:

To find the peak charging I_{OL} assume that the gate is initially charged the steady-state value of V_{EE}. Therefore apply the following relationship.

$$RG = \frac{[V_{OH}@650\mu A-(V_{OL}+V_{EE})]}{IOL,PEAK} = \frac{[V_{CC2}-1-(V_{OL}+V_{EE})]}{IOL,PEAK} = \frac{18V-1V-(1.5V+(-5V))}{2.0A}$$

= 10.25Ω

= 10.5Ω (for a 1% resistor)

(Note from Figure 72 that the real value of I_{OL} may vary from the value calculated from the simple model

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shown.)

Step2: Calculate total power dissipation in the ICPL-316J:

The ICPL-316J total power dissipation (P_T) is equal to the sum of the input-side power (P_I) and output-side power (P_O):

$P_T = P_I + P_O$; $P_I = I_{CC1} * V_{CC1}$

$P_O = P_{O(BIAS)} + P_{O,SWTICH}$

$= I_{CC2} * (V_{CC2} – V_{EE}) + E_{SWITCH} * f_{SWITCH}$

$P_{O(BIAS)}$ = steady-state power dissipation in the ICPL-316J due to biasing the device.

$P_{O(SWITCH)}$ = transient power dissipation in the ICPL-316J due to charging and discharging power device gate.

E_{SWITCH} = Average Energy dissipated in ICPL-316J due to switching of the power device over one switching cycle (μJ/cycle).

f_{SWITCH} = average carrier signal frequency

For R_G = 10.5, the value read from Figure 73 is E_{SWITCH}= 6.05 μJ. Assume a worst-case average I_{CC1} = 16.5 mA (which is given by the average of I_{CC1H} and I_{CC1L}). Simiarly the average I_{CC2} = 5.5 mA

P_I = 16.5 mA * 5.5 V = 90.8 mW

$P_O = P_{O(BIAS)} + P_{O,SWITCH}$

= 5.5 mA * (18 V – (–5 V)) + 6.051 μJ * 15 kHz

= 126.5 mW + 90.8 mW

= 217.3 mW

Step 3: Compare the calculated power dissipation with the absolute maximum values for the ICPL-316J:

For the example,

P_I = 90.8 mW < 150 mW (abs. max.) OK

P_O = 217.3 mW < 600 mW (abs. max.) OK

Therefore, the power dissipation absolute maximum rating has not been exceeded for the example.

Please refer to the following Thermal Model section for an explanation on how to calculate the maximum junction temperature of the ICPL-316J for a given PC board layout configuration.

Fig.72 Typical peak ION and IOFF currents vs. Rg (for Pswitch ICPL-316J output driving an IGBT rated at 600 V/100 A)

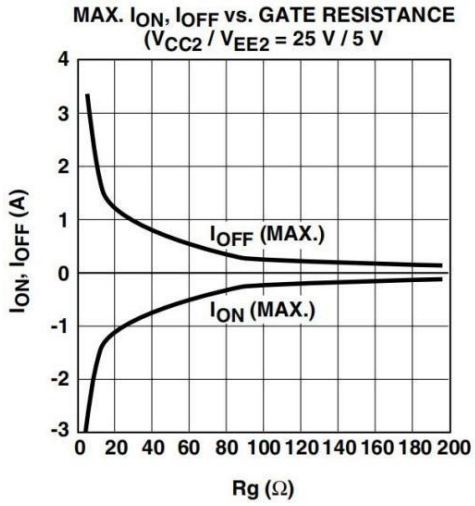
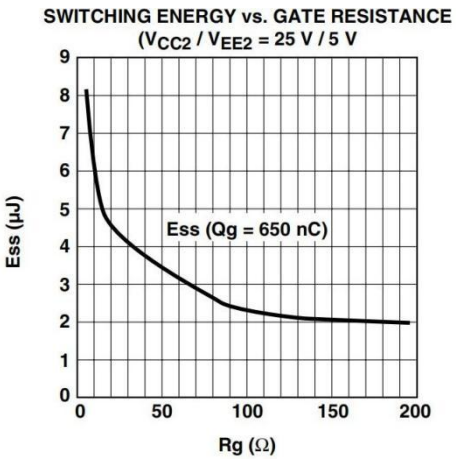


Fig.73 Switching energy plot for calculating average (for ICPL-316J output driving an IGBT rated at 600 V/100 A)



Thermal Model

The ICPL-316J is designed to dissipate the majority of the heat through pins 4 for the input IC and pins 9 and 10 for the output IC. (There are two V_{EE} pins on the output side, pins 9 and 10, for this purpose.) Heat flow through other pins or through the package directly into ambient are considered negligible and not modeled

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here.
In order to achieve the power dissipation specified in the absolute maximum specification, it is imperative that pins 4, 9, and 10 have ground planes connected to them. As long as the maximum power specification is not exceeded, the only other limitation to the amount of power one can dissipate is the absolute maximum junction temperature specification of 125°C. The junction temperatures can be calculated with the following equations:

$T_{ji} = P_i (q_{i4} + q_{4A}) + T_a$

$T_{jo} = P_o (q_{o9,10} + q_{9,10A}) + T_a$

Where P_i = power into input IC and Po = power into output IC. Since q_{4A} and $q_{9,10A}$ are dependent on PCB layout and airflow, their exact number may not be available. Therefore, a more accurate method of calculating the junction temperature is with the following equations:

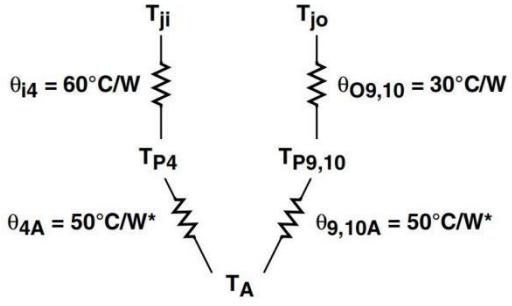
$T_{ji} = P_{iq_{i4}} + T_{P4}$

$T_{jo} = P_{oq_{o9,10}} + T_{P9,10}$

These equations, however, require that the pin 4 and pins 9, 10 temperatures be measured with a thermal couple on the pin at the ICPL-316J package edge.
From the earlier power dissipation calculation example:
P_i = 90.8 mW, Po = 314 mW, T_A = 100°C, and assuming the thermal model shown in Figure 73 below.
T_{ji} = (90.8 mW)(60°C/W + 50°C/W) + 100°C = 110°C
T_{jo} = (240 mW)(30°C/W + 50°C/W) + 100°C = 119°C
Both of which are within the absolute maximum specification of 125°C.
If we, however, assume a worst case PCB layout and no air flow where the estimated q_{4A} and $q_{9,10A}$ are 100°C/W. Then the junction temperatures become:
T_{ji} = (90.8 mW)(60°C/W + 100°C/W) + 100°C = 115°C
T_{ji} = (240 mW)(30°C/W + 100°C/W) + 100°C = 131°C
The output IC junction temperature exceeds the abso- lute maximum specification of 125°C. In this case, PCB layout and airflow will need to be designed so that the junction temperature of the output IC does not exceed 125°C.
If the calculated junction temperatures for the thermal model in Figure 74 is higher than 125°C, the pin temperature for pins 9 and 10 should be measured (at the package edge) under worst case operating environment for a more accurate estimate of the junction temperatures.

T_{ji} = junction temperature of input side IC T_{jo} = junction temperature of output side IC T_{P4} = pin 4 temperature at package edge
$T_{P9,10}$ = pin 9 and 10 temperature at package edge
θ_{I4} = input side IC to pin 4 thermal resistance
$\theta_{I9,10}$ = output side IC to pin 9 and 10 thermal resistance
θ_{4A} = pin 4 to ambient thermal resistance
$\theta_{9,10A}$ = pin 9 and 10 to ambient thermal resistance
*The θ_{4A} and $\theta_{9,10A}$ values shown here are for PCB layouts shown in Figure 74 with reasonable air flow. This value may increase or decrease by a factor of 2 depending on PCB layout and air flow.

Fig.74 ICPL-316J thermal model



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Printed Circuit Board Layout Considerations

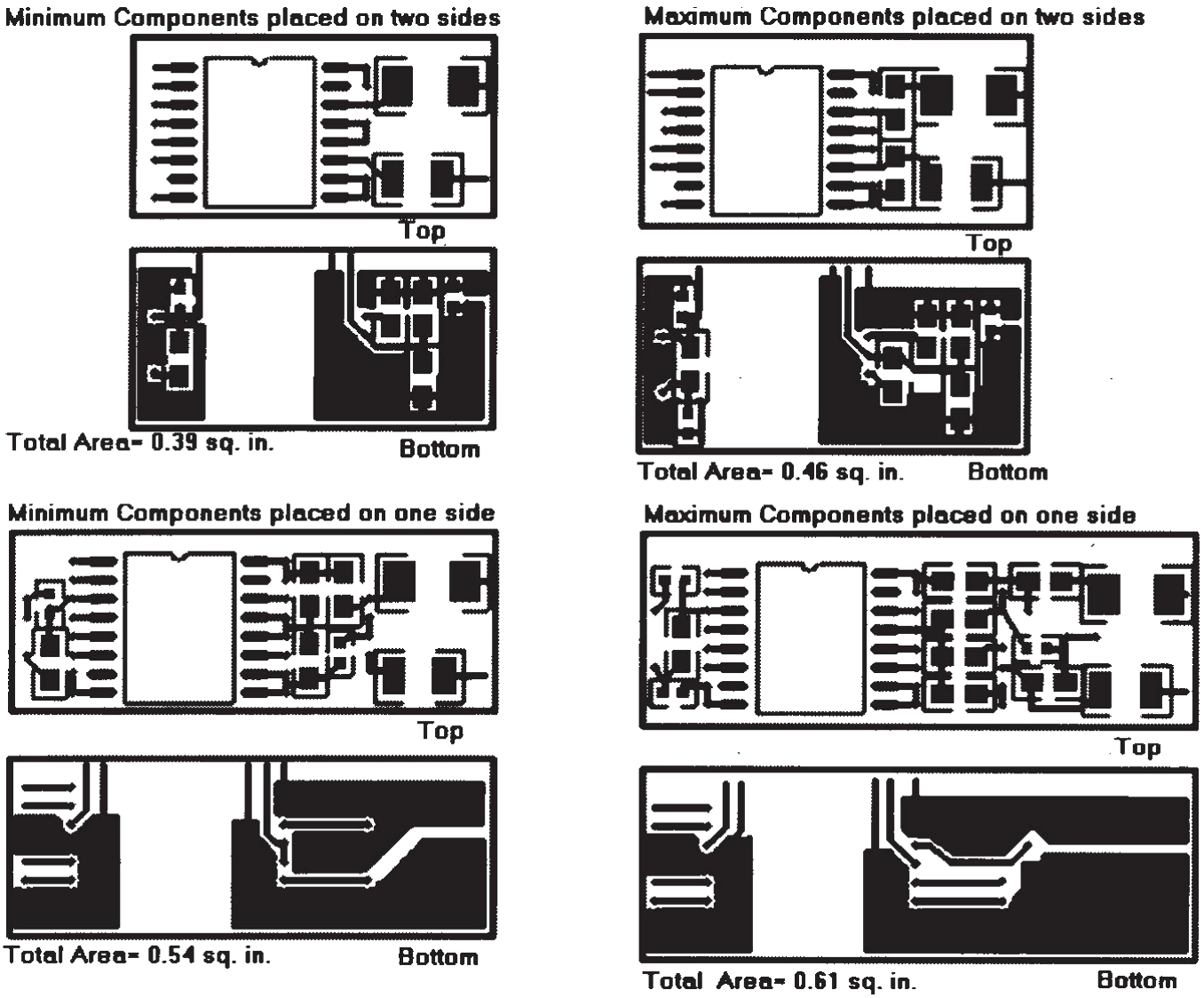
Adequate spacing should always be maintained between the high voltage isolated circuitry and any input referenced circuitry. Care must be taken to provide the same minimum spacing between two adjacent high-side isolated regions of the printed circuit board. Insufficient spacing will reduce the effective isolation and increase parasitic coupling that will degrade CMR performance.

The placement and routing of supply bypass capacitors requires special attention. During switching transients, the majority of the gate charge is supplied by the bypass capacitors. Maintaining short bypass capacitor trace lengths will ensure low supply ripple and clean switching waveforms.

Ground Plane connections are necessary for pin 4 (GND1) and pins 9 and 10 (V_{EE}) in order to achieve maximum power dissipation as the ICPL-316J is designed to dissipate the majority of heat generated through these pins. Actual power dissipation will depend on the application environment (PCB layout, air flow, part placement, etc.) See the Thermal Model section for details on how to estimate junction temperature.

The layout examples below have good supply bypassing and thermal properties, exhibit small PCB footprints, and have easily connected signal and supply lines. The four examples cover single sided and double sided component placement, as well as minimal and improved performance circuits.

Fig.75 Recommended layout(s).



System Considerations

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Propagation Delay Difference (PDD)

The ICPL-316J includes a Propagation Delay Difference (PDD) specification intended to help designers minimize “dead time” in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 59) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails, a potentially catastrophic condition that must be prevented.

To minimize dead time in a given design, the turn-on of the ICPL-316J driving Q2 should be delayed (relative to the turn- off of the ICPL-316J driving Q1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 76. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 400 ns over the operating temperature range of -40°C to 100°C.

Delaying the ICPL-316J turn-on signals by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 77. The maximum dead time for the ICPL-316J is 800 ns (= 400 ns - (-400 ns)) over an operating temperature range of -40°C to 100°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

Fig. 76 Minimum LED Skew for Zero Dead Time

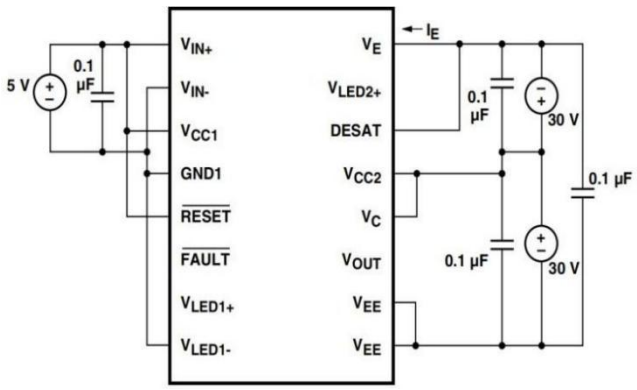
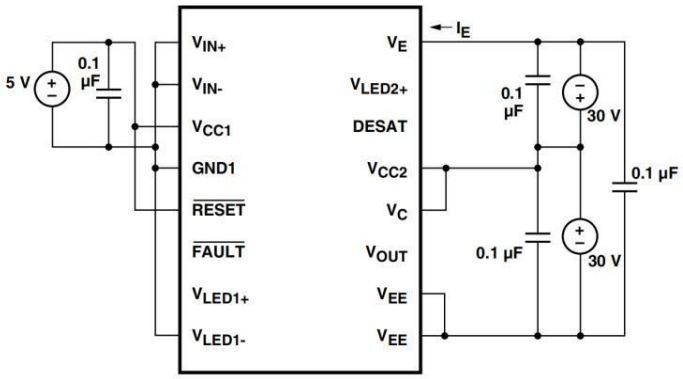


Fig.77 Waveforms for Dead Time Calculation



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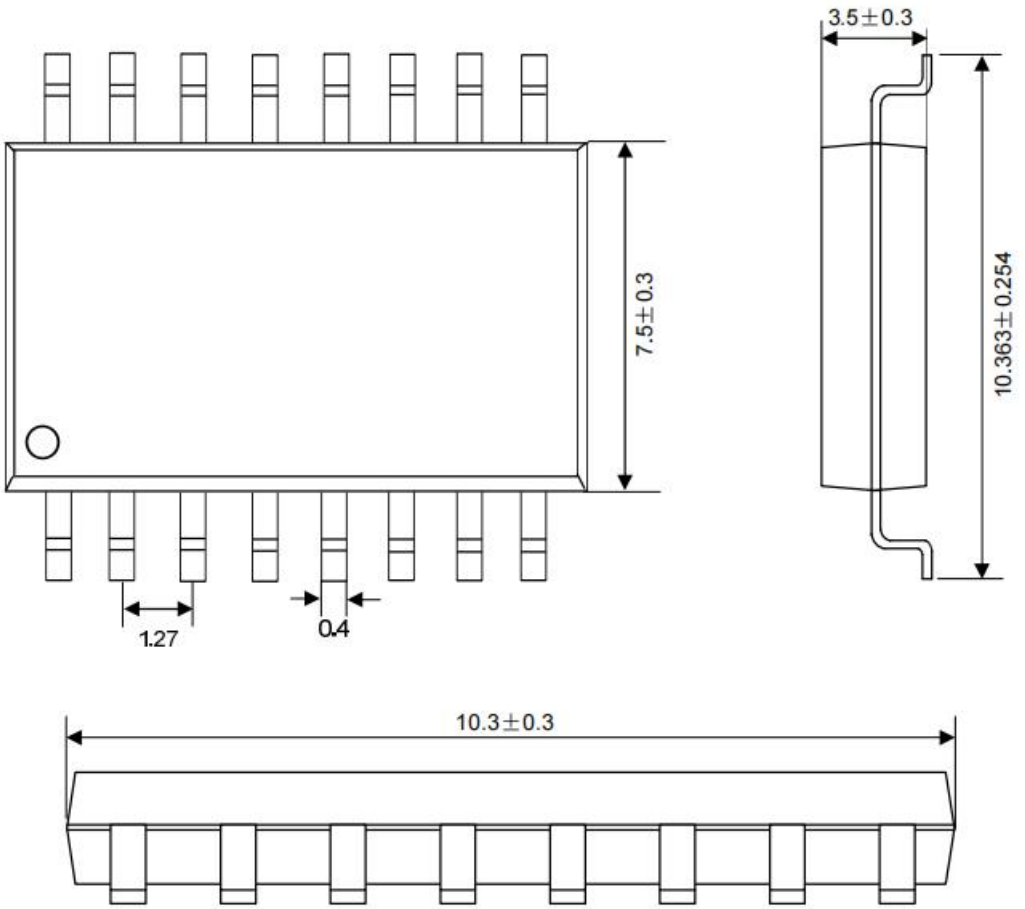
PACKAGE DIMENSIONS

Option SOP16



- **Dimensions in mm unless otherwise stated**

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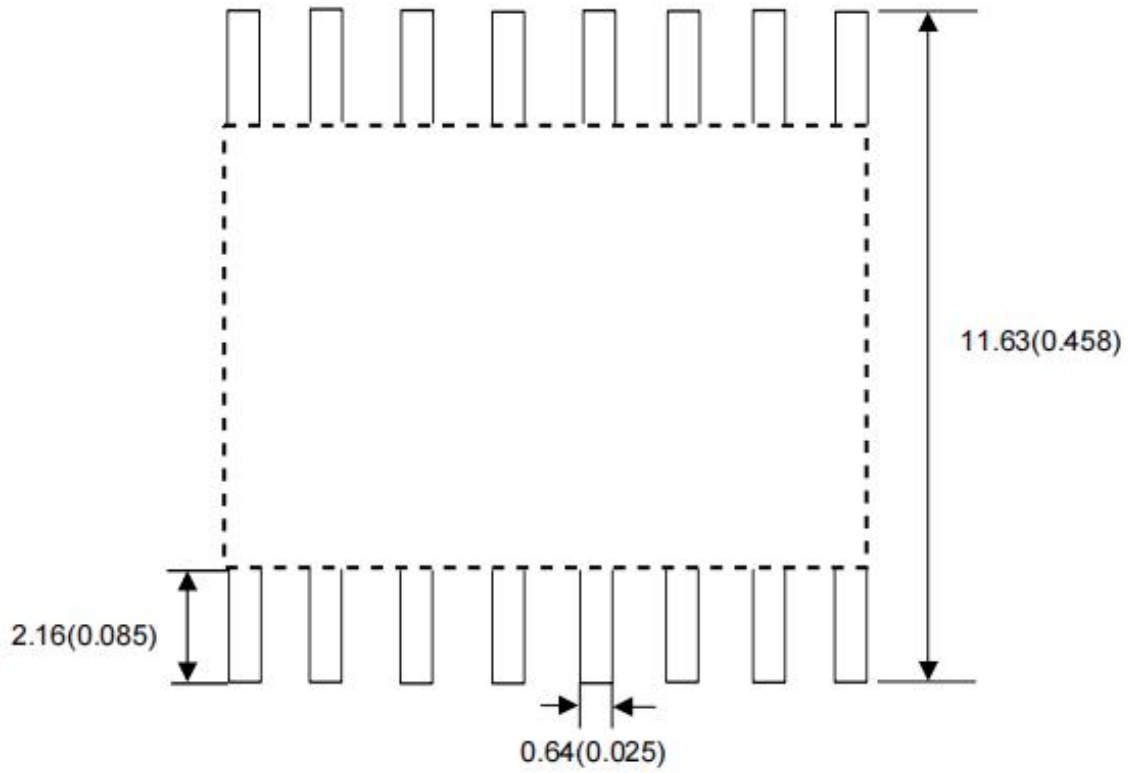
RECOMMENDED SOLDER MASK

Surface Mount (Low Profile) Lead Forming



- **Dimensions in mm unless otherwise stated**

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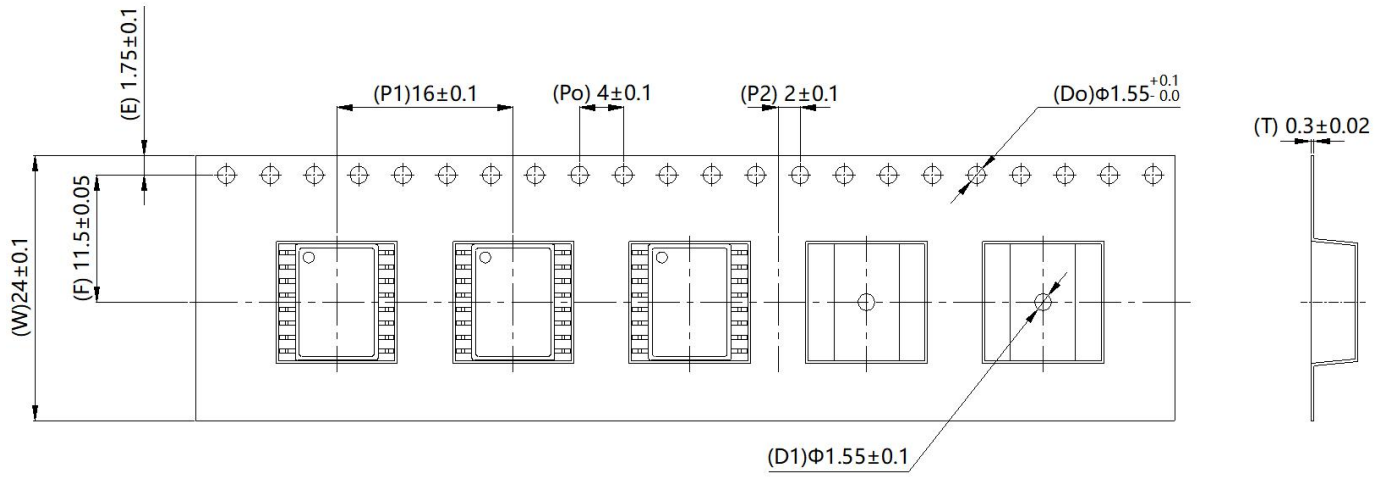
CARRIER TAPE SPECIFICATIONS

Option SOP16



- **Dimensions in mm unless otherwise stated**

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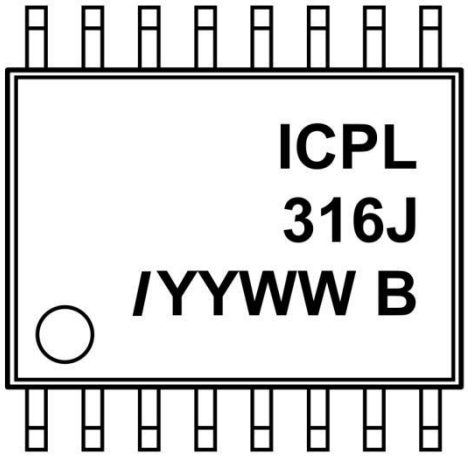
ORDERING AND MARKING INFORMATION

Marking Information



ICPL	:	Company Abbr.
316J	:	Part Number
/	:	ISOMICRON
YY	:	Fiscal Year
WW	:	Work Week
B	:	Manufacturing Code

Order Code

ICPL – 316 J - 5 0 0 E

Company Abbr.

Part Number

Lead Forming
5: SM-SL

Halogen Free
E: Halogen-free,Lead-free
Z: Halogen, Lead-free

None

Performance
0: Normal
1: Enhanced
2: Industrial level
3: Auto level
4: Military level

Packing Quantity

Option	Quantity	Quantity – Inner box	Quantity – Outer box
SM-SL	850 Units/Reel	2 Reels/Inner box	5 Inner box/Outer box = 8500 Units

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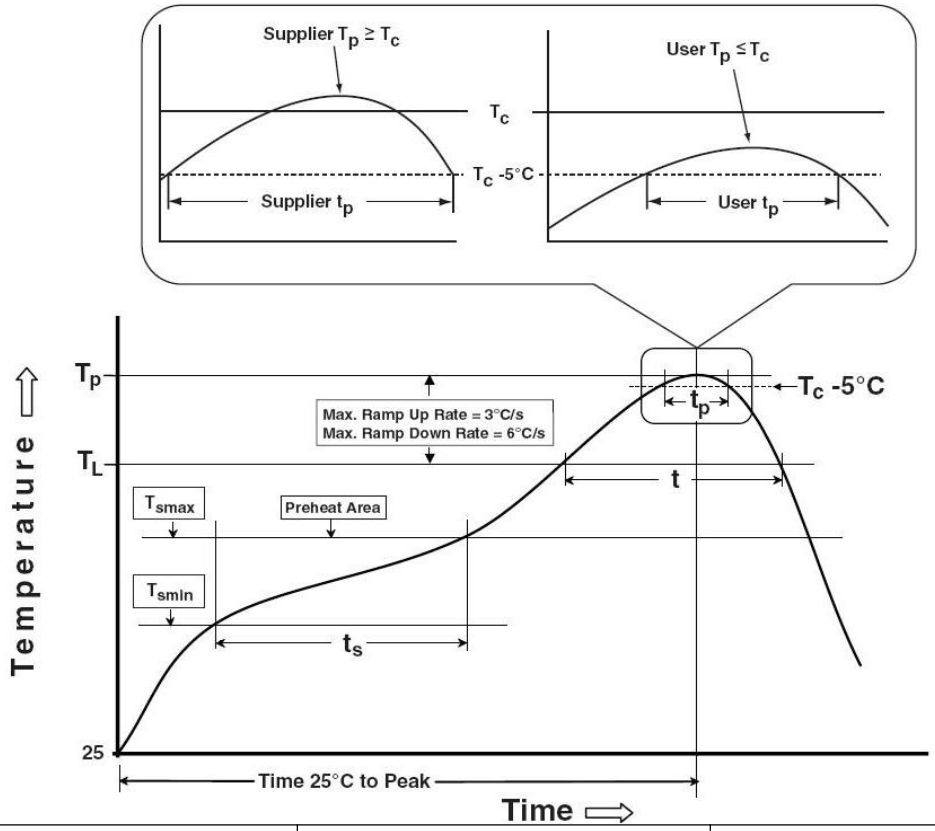
REFLOW INFORMATION

Reflow Profile



Profile Feature	Sn-Pb Assembly Profile	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	100	150°C
Temperature Max. (Tsmax)	150	200°C
Time (ts) from (Tsmin to Tsmax)	60-120 seconds	60-120 seconds
Ramp-up Rate (tL to tP)	3°C/second max.	3°C/second max.
Liquidous Temperature (TL)	183°C	217°C
Time (tL) Maintained Above (TL)	60 – 150 seconds	60 – 150 seconds
Peak Body Package Temperature	235°C +0°C / -5°C	260°C +0°C / -5°C
Time (tP) within 5°C of 260°C	20 seconds	30 seconds
Ramp-down Rate (TP to TL)	6°C/second max	6°C/second max
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

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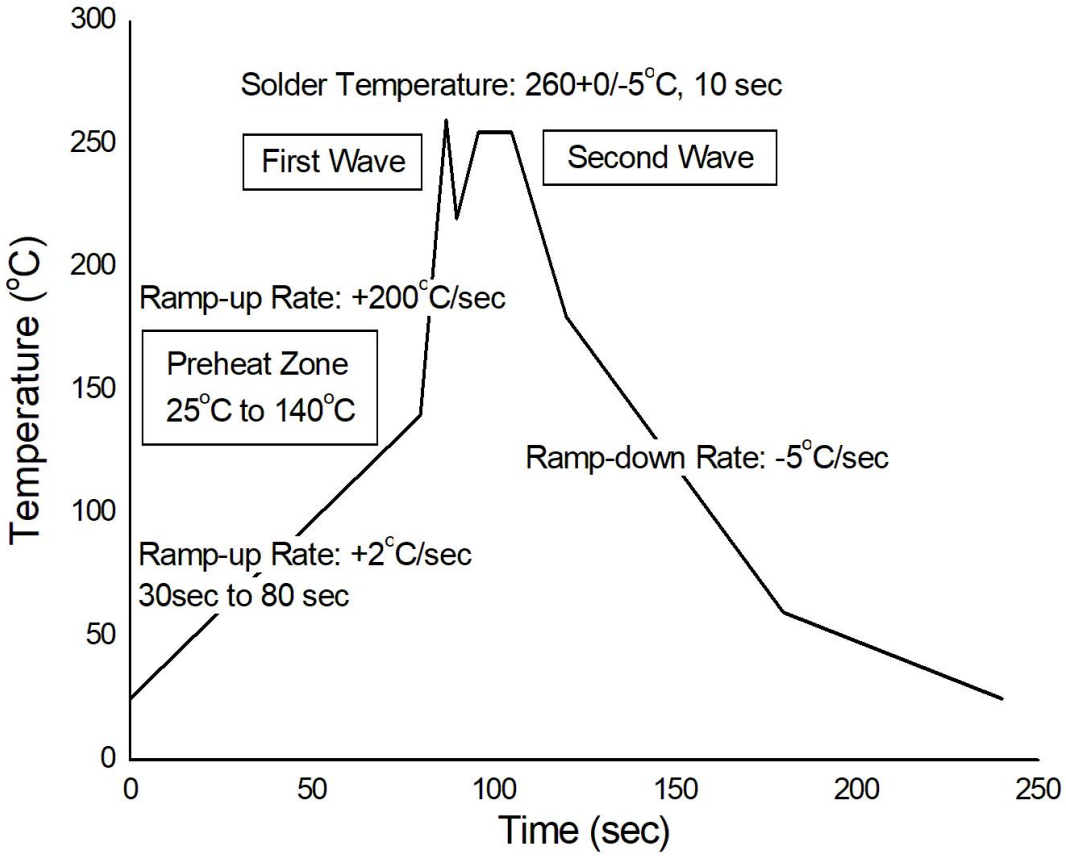
TEMPERATURE PROFILE OF SOLDERING

Wave Soldering (JESD22-A111 Compliant)



Hand Soldering By Soldering Iron	
Soldering Temperature	380+0/-5°C
Soldering Time	3 sec max.

- **One time soldering is recommended for all soldering method.**
- **Do not solder more than three times for IR reflow soldering.**

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- Please contact ISOMICRON sales agent for special application request.
- Immerge unit's body in solder paste is not recommended.
- Parameters provided in datasheets may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated in each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify ISOMICRON's terms and conditions of purchase, including but not limited to the warranty expressed therein.
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