

NEOFIDELITY

# NTP8818

High Performance, High Fidelity Power Driver Integrated Full Digital Audio Amplifier

Datasheet  
ver. 1.2

CONFIDENTIAL

## General Description

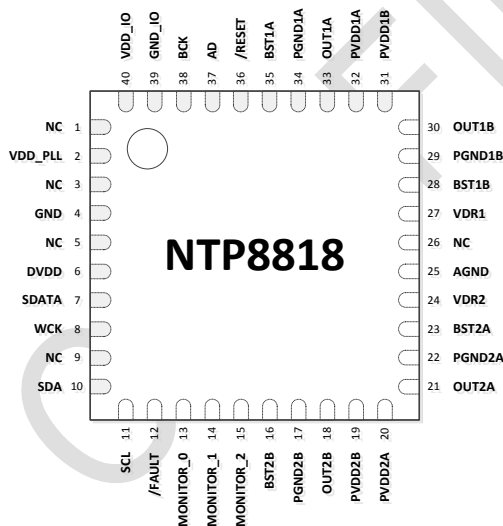
The NTP8818 is a single chip full digital audio amplifier including power stage for stereo amplifier system. NTP8818 is integrated with versatile digital audio signal processing functions, high-performance, high-fidelity fully digital PWM modulator and two high-power full-bridge MOSFET power stages.

The NTP8818 receives digital serial audio data with sampling frequencies of 32kHz, 44.1kHz, 48kHz, and 96kHz. It delivers 2 x 20 watts in stereo mode without heat sink.

The NTP8818 has a mixer and Bi-Quad filters which can be used to implement the essential audio signal processing functions like loudness control, compensation of a loud speaker response and parametric equalization.

All the functions of the NTP8818 can be controlled by internal register values via I<sup>2</sup>C host interface bus.

## Package



( 40 pin SAW QFN 6mm x 6mm Package )

## Features

- 2 CH Stereo (15W x 2 BTL)
- Wide Operating Supply Voltage Range (7V to 20V)
- SDATA Generator (I<sup>2</sup>S output)
- Floating Point Operation
- 24 Programmable Bi-Quad Filters
  - ✓ Speaker Compensation
  - ✓ LPF, HPF, DC Cut
  - ✓ Advanced Parametric Equalizer
- 3 Band Dynamic Range Control
- Loudness Control
- Protection Circuit
  - ✓ OCP(Over Current Protection)
  - ✓ OTP(Over Temperature Protection)
  - ✓ UVP(Under Voltage Protection)
  - ✓ BQ/DRC Check Sum
- Vol/Soft Mute/Power Meter/NS Feedback
- Smart PWM Switch on/off
- High Efficiency
- DC protection
  - ✓ DC cut filter
  - ✓ Coefficient memory checksum
  - ✓ Modulation Index check

## Applications

- LCD/OLED/UHD/FUD TV or Monitor TV
- Docking Station
- Mini-Component Audio Solution

## Ordering Information

| Product ID | Package Type | Pin | Size    |
|------------|--------------|-----|---------|
| NTP8818    | SAW QFN      | 40  | 6 x 6mm |

### Disclaimer

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## 1. BLOCK DIAGRAM

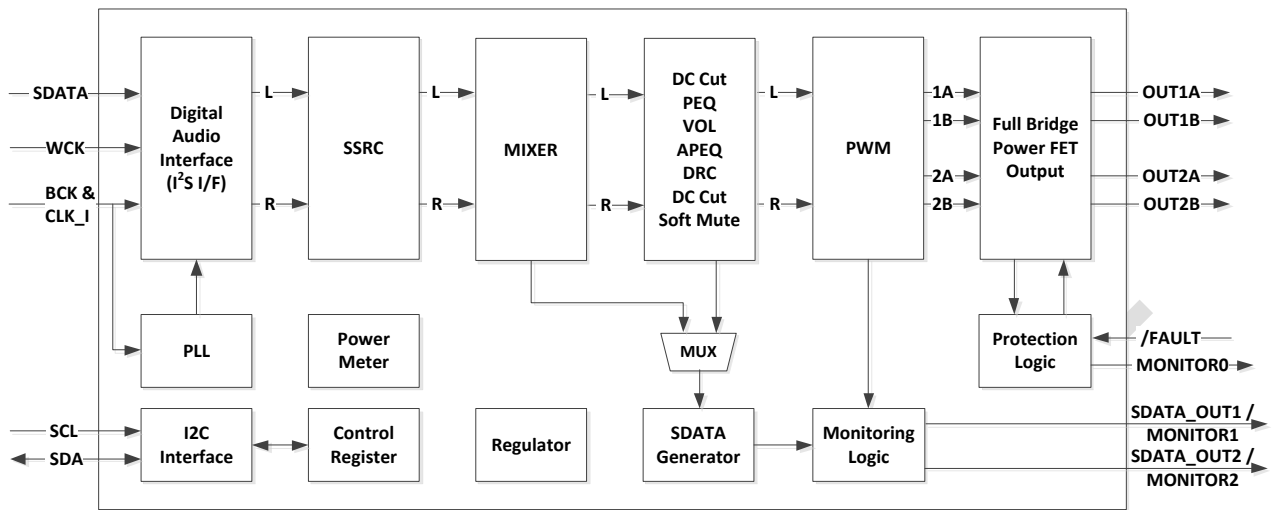


Figure 1. NTP8818 Block Diagram

## 2. PIN ASSIGNMENTS

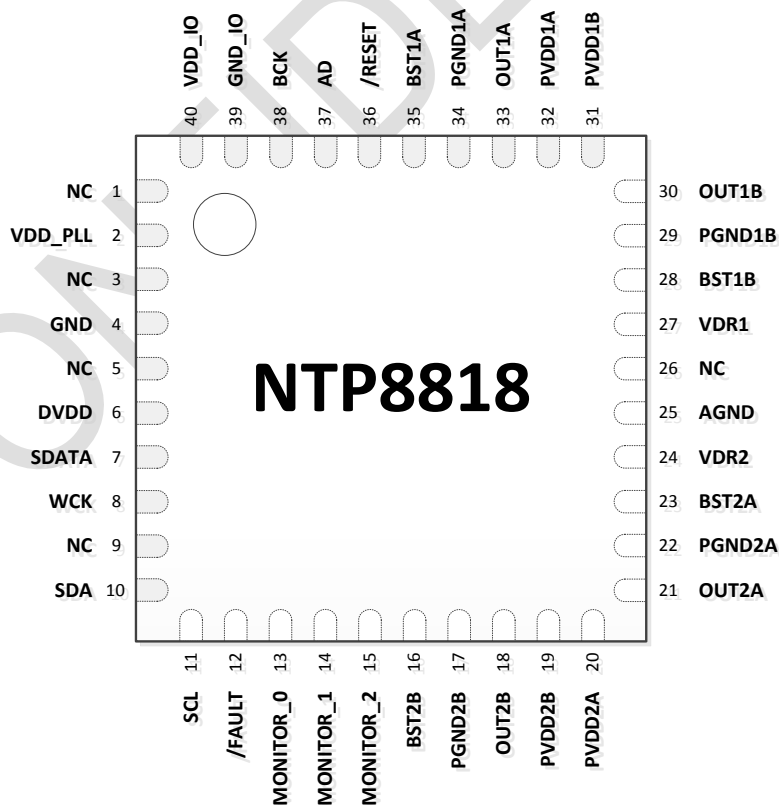


Figure 2. NTP8818 Pin Assignments

### 3. PIN DESCRIPTIONS

| PIN | NAME        | TYPE | DESCRIPTION   |
|-----|-------------|------|---|
| 1   | NC          | -    | Not connected   |
| 2   | VDD_PLL     | P    | Regulator output for PLL digital block, 1.2V                                      |
| 3   | NC          | -    | Not connected   |
| 4   | GND         | P    | This pin should be connected to Ground  |
| 5   | NC          | -    | Not connected   |
| 6   | DVDD        | P    | Regulator output for Core block, 1.2V   |
| 7   | SDATA       | I    | I <sup>2</sup> S serial data input  |
| 8   | WCK         | I    | I <sup>2</sup> S word clock   |
| 9   | NC          | -    | Not connected   |
| 10  | SDA         | I/O  | I <sup>2</sup> C data   |
| 11  | SCL         | I    | I <sup>2</sup> C clock  |
| 12  | /FAULT      | I    | Active low to reset internal power stage, Pull-up                                 |
| 13  | MONITOR_0   | O    | No Connection, monitoring signal out from protection logic                        |
| 14  | MONITOR_1   | O    | monitoring signal out from processor block / I <sup>2</sup> S output (SDATA word) |
| 15  | MONITOR_2   | O    | monitoring signal out from processor block / I <sup>2</sup> S output (SDATA word) |
| 16  | BST2B       | P    | Bootstrap supply, external capacitor to OUT2B is required                         |
| 17  | PGND2B      | P    | Ground  |
| 18  | OUT2B       | O    | Power stage PWM output 2B   |
| 19  | PVDD2B      | P    | Power supply for PWM Power stage 2B   |
| 20  | PVDD2A      | P    | Power supply for PWM Power stage 2A   |
| 21  | OUT2A       | O    | Power stage PWM output 2A   |
| 22  | PGND2A      | P    | Ground  |
| 23  | BST2A       | P    | Bootstrap supply, external capacitor to OUT2A is required                         |
| 24  | VDR2        | P    | Gate drive voltage regulator decoupling pin, capacitor to GND is required         |
| 25  | AGND        | P    | Ground  |
| 26  | NC          | -    | Not connected   |
| 27  | VDR1        | P    | Gate drive voltage regulator decoupling pin, capacitor to GND is required         |
| 28  | BST1B       | P    | Bootstrap supply, external capacitor to OUT1B is required                         |
| 29  | PGND1B      | P    | Ground  |
| 30  | OUT1B       | O    | Power stage PWM output 1B   |
| 31  | PVDD1B      | P    | Power supply for PWM Power stage 1B   |
| 32  | PVDD1A      | P    | Power supply for PWM Power stage 1A   |
| 33  | OUT1A       | O    | Power stage PWM output 1A   |
| 34  | PGND1A      | P    | Ground  |
| 35  | BST1A       | P    | Bootstrap supply, external capacitor to OUT1A is required                         |
| 36  | /RESET      | I    | Active low to reset NTP8818, Schmitt trigger input                                |
| 37  | AD          | I    | I <sup>2</sup> C device address selection   |
| 38  | BCK         | I    | System master clock, Schmitt trigger input  |
| 39  | GND_IO      | P    | Ground for digital interface I/O  |
| 40  | VDD_IO      | P    | Power supply for digital interface I/O, 3.3V                                      |
| -   | Thermal Pad | P    | This pad should be connected to Ground  |

P = Power or Ground, I = Input, O = Output, I/O = Input / Output

Table 1. NTP8818 Pin Description

## 4. CHARACTERISTICS AND SPECIFICATIONS

### 4.1. Absolute Maximum Ratings

| Parameter                     | Reference      | Rating        | Unit |
|-------------------------------|----------------|---------------|------|
| DVDD voltage                  | DGND           | -0.3 ~ 1.5    | V    |
| VDD_IO voltage                | GND_IO         | -0.3 ~ 5.25   | V    |
| Logic input voltage           | GND            | -0.3 ~ 5.25   | V    |
| Logic output voltage          | GND            | -0.3 ~ 5.25   | V    |
| PVDDXX voltage                | PGNDXX         | 24            | V    |
| OUTXX voltage                 | PGNDXX         | -0.3 ~ PVDDXX | V    |
| BSTXX voltage                 | PGNDXX         | 30            | V    |
| VDRX voltage                  | PGNDXX         | 6.0           | V    |
| Operating Ambient Temperature | T <sub>A</sub> | -25 ~ +85     | °C   |
| Junction temperature          | T <sub>J</sub> | 150           | °C   |

### 4.2. Recommended Operating Conditions

| Parameter      | Reference | Rating    | Unit |
|----------------|-----------|-----------|------|
| VDD_IO voltage | GND_IO    | 3.0 ~ 3.6 | V    |
| PVDDXX voltage | PGNDXX    | 7 ~ 20    | V    |
| VDRX voltage   | PGNDXX    | 4.7 ~ 5.6 | V    |

### 4.3. DC Electrical Characteristics

| Parameter  | Symbol           | Condition                                       | Min  | Typ  | Max  | Unit |
|--|------------------|---|------|------|------|------|
| <b>Logic Block</b> (VDD_IO=3.3V, T <sub>A</sub> =+25°C, unless otherwise specified.) |                  |   |      |      |      |      |
| Input High voltage   | V <sub>IH</sub>  | -   | 2.08 |      |      | V    |
| Input Low voltage  | V <sub>IL</sub>  | -   | -0.3 |      | 0.89 | V    |
| Schmitt trig. Hysteresis   | ΔV               | -   |      | 0.29 |      | V    |
| Input current  | I <sub>I</sub>   | V <sub>IN</sub> =V <sub>IL</sub> MAX, DVDD=MIN  | -50  |      |      | μA   |
|  |                  | V <sub>IN</sub> =V <sub>IH</sub> MIN, DVDD=MIN  |      |      | 50   | μA   |
| Input leakage current  | I <sub>L</sub>   | V <sub>IN</sub> =VSS, DVDD=MIN                  | -10  |      | 10   | μA   |
| Output Low voltage   | V <sub>OL</sub>  | I <sub>OL</sub> = -4mA                          | 0    |      | 0.4  | V    |
| Output High voltage  | V <sub>OH</sub>  | I <sub>OH</sub> = 4mA                           | 2.4  |      | 3.6  | V    |
| LDO output voltage   | V <sub>LDO</sub> | DVDD  | 1.08 |      | 1.32 | V    |
| <b>Driver Block</b> (PVDDXX=13V, T <sub>A</sub> =+25°C, unless otherwise specified.) |                  |   |      |      |      |      |
| Current consumption  |                  | VDD_IO=3.3V, No Input, No Load                  |      | 23   |      | mA   |
|  |                  | PVDD=13V, No Input, 8 Ω Load with 10uH inductor |      | 30   |      |      |
| Peak current limit   | OCP              | -   |      | 6    |      | A    |
| Thermal shutdown temperature   | OTP              |   | 140  | 150  | 160  | °C   |
| Under voltage lockout  | UVP              |   | 4.75 | 5.0  | 5.5  | V    |

### 4.4. Performance Specification

#### Speaker Amplifier

| Parameter  | Condition                 | Min | Typ | Max | Unit |
|------------|---------------------------|-----|-----|-----|------|
| SNR        | AES17, A-weighting filter |     | 96  |     | dB   |
| THD+N      | 1W, 1kHz @PVDD 18V        |     | 0.1 |     | %    |
| Cross talk | Dolby standard            |     | 70  |     | dB   |

### 4.5. Switching Characteristics – I<sup>2</sup>C Control

| Parameter                          | Symbol             | Condition | Min  | Max | Unit |
|------------------------------------|--------------------|-----------|------|-----|------|
| <b>I<sup>2</sup>C Control Port</b> |                    |           |      |     |      |
| SCL clock frequency                | F <sub>scl</sub>   |           | -    | 400 | kHz  |
| Hold time for START condition      | T <sub>hdsta</sub> |           | 600  | -   | ns   |
| Low period of the SCL clock        | T <sub>low</sub>   |           | 1300 | -   | ns   |
| High period of the SCL clock       | T <sub>high</sub>  |           | 600  | -   | ns   |
| Rise time of SDA and SCL signals   | T <sub>rise</sub>  |           | -    | 300 | ns   |
| Fall time of SDA and SCL signals   | T <sub>fall</sub>  |           | -    | 300 | ns   |
| Setup time for STOP condition      | T <sub>susto</sub> |           | 600  | -   | ns   |

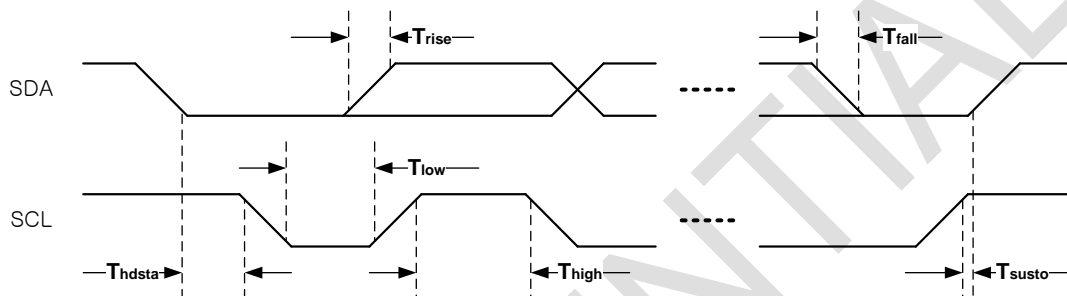


Figure 3. I<sup>2</sup>C Mode Timing

### 4.6. Switching Characteristics – Audio Interface

| Parameters                              | Symbol   | Min | Max | Unit |
|---|--|-----|-----|------|
| BCK high time                           | t <sub>bh</sub>                                    | 20  | -   | ns   |
| BCK low time                            | t <sub>bl</sub>                                    | 20  | -   | ns   |
| SDATA setup time before BCK rising edge | t <sub>ds</sub>                                    | 10  | -   | ns   |
| SDATA hold time after BCK rising edge   | t <sub>dh</sub>                                    | 10  | -   | ns   |
| WCK setup time before BCK rising edge   | t <sub>ws</sub>                                    | 20  | -   | ns   |
| BCK rising edge before WCK edge         | t <sub>wh</sub>                                    | 20  | -   | ns   |
| BCK falling edge before WCK edge        | t <sub>wl</sub>                                    | -20 | 20  | ns   |
| Rising/Falling time for BCK/WCK         | t <sub>br</sub> /t <sub>bf</sub> /t <sub>wrf</sub> | -   | 50  | ns   |

※ Schmitt trigger characteristics (V<sub>SIH</sub> Min = 1.85V, V<sub>SIH</sub> Max = 0.9V)

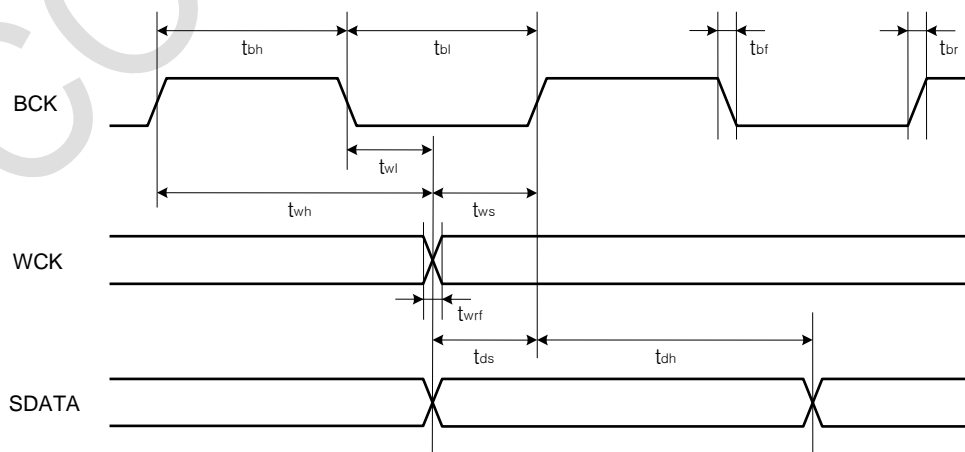


Figure 4. Audio Interface Timing

## 5. I<sup>2</sup>C BUS OF NTP8818

The NTP8818 uses an industry standard Inter IC Control (I<sup>2</sup>C) bus to communicate with host IC. A host IC can write or read internal registers of the NTP8818 via the I<sup>2</sup>C bus.

### 5.1. General Description of I<sup>2</sup>C Bus

The I<sup>2</sup>C bus uses two signal lines – a serial clock line (SCL) and a serial data line (SDA). Because the SDA line is open-drain type port, both the NTP8818 and a host IC can only drive these pins low or leave them open.

In I<sup>2</sup>C bus, a master device means the device which generates serial clock on the SCL. A slave device means the device which receives serial clock. There can be many master and slave devices on an I<sup>2</sup>C bus. But, when one master device works on the bus, the other master devices should not generate signal on the lines. These unexpected interrupts can make other slave devices to fail to communicate with the mater device.

The NTP8818 supports only slave mode of I<sup>2</sup>C bus. So, the NTP8818 always receives serial clock from a host IC. The slave mode is enough to write/read data to/from the NTP8818.

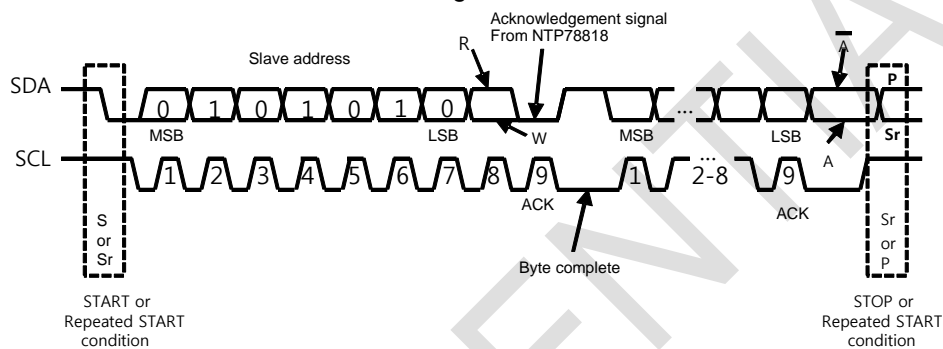


Figure 5. Basic Signaling Elements of I<sup>2</sup>C Bus

If there are no communication on I<sup>2</sup>C bus, lines must keep in high state. I<sup>2</sup>C bus begins communication with the start condition and ends communication with the stop condition. The start condition can be generated by changing the SDA state high to low, during the SCL state remains in high. The stop condition can be generated by changing the SDA state low to high during the SCL remains in high state. Be aware that the stop condition always reset the internal status of I<sup>2</sup>C bus control logic. Except these two conditions, the SDA may not change during the SCL in high state. Otherwise, abnormal start or stop condition will be generated.

I<sup>2</sup>C bus transfers the MSB of a byte on 1st data slot and the LSB of a byte on 8th data slot. I<sup>2</sup>C bus checks success or fail of transfer on every 1 byte transfer. The device which found an expected data on SDA must generate acknowledgement (keep low on SDA) on 9th clock. If there is no acknowledgement on 9th clock, the device which generated a data on SDA may stop transfer. The NTP8818 will generate acknowledgement for every successful data transfer of 1 byte in write mode. But, in read mode, because data is generated by the NTP8818, the NTP8818 will not generate an acknowledgement. In this case, on the contrary, the NTP8818 will check SDA state on 9th clock that the master device received a read data properly.

Last 8th bit of the 1st byte is used to indicate whether the master device want to write or read data

#### 5.1.1. Writing Operation

When last 8th bit of the 1st byte is set to low state, the writing operation of I<sup>2</sup>C bus begins. The NTP8818 supports 3 kind of writing operations which presented on **Figure 6**.

The type presented on **Figure 6-(a)** is single byte write operation. “Sub address” on 2nd byte means the internal register address of the NTP8818. The “Data” on 3rd byte will be written into the internal register address on “Sub address”. If stop condition is not generated, writing “data” on specific “sub address” can be repeated like **Figure 6-(b)**. “Data #n” will be written on “sub address #n”.

The type presented on **Figure 6-(c)** is single byte write operation under address auto increment mode. The AIF on 1st bit of 2nd byte is the address auto increment flag. If SDA is set to high state on AIF slots, the NTP8818 write data continuously with register addresses



which increased from initial “sub address” for every byte; “Data #n” will be written on “sub address” + n – 1. The internal address will cycle automatically.

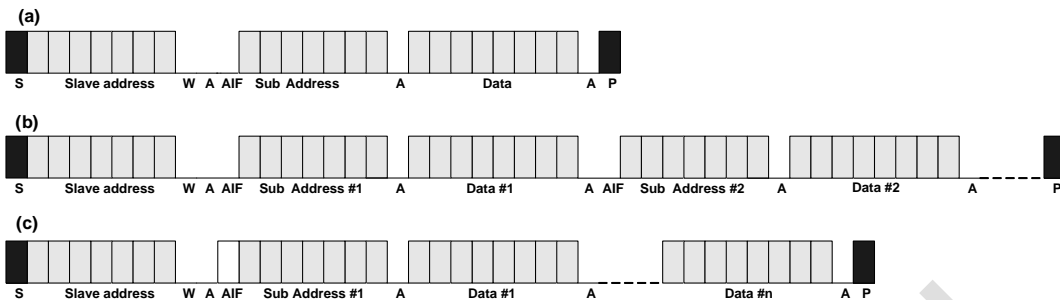


Figure 6. Single Byte Write Mode Sequence

Figure 7-(a), Figure 7-(b), and Figure 7-(c) represent 4 byte writing operations. Coefficient Mode Register address 0x00~0x5B are used to configure Bi-Quad filter coefficients, those are BQ, QMF\_BQ, Loudness filter gain, attack gain, power meter gain and BQ/DRC check. The data size of these coefficients and gains is 4 byte for each. The difference between 4byte writing operation and single byte writing operation is only the size of transferring data. So, after sending “Sub address”, 4 sequential bytes must be transferred from the MSB(most significant byte) to the LSB(least significant byte) sequence.

The type presented on Figure 7-(c) is quad byte write operation under address auto increment mode, AIF function. Please compare the data transfer size between Figure 6 and Figure 7.

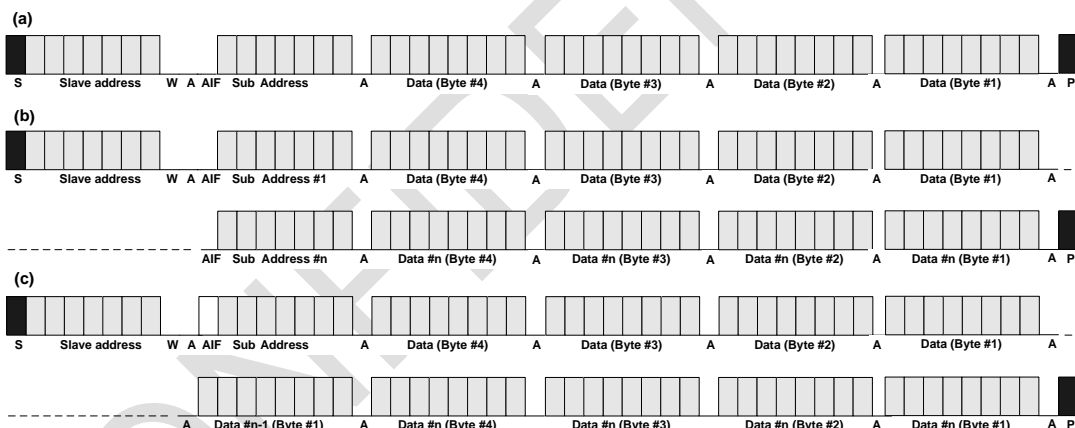


Figure 7. Quad Byte Write Mode Sequence

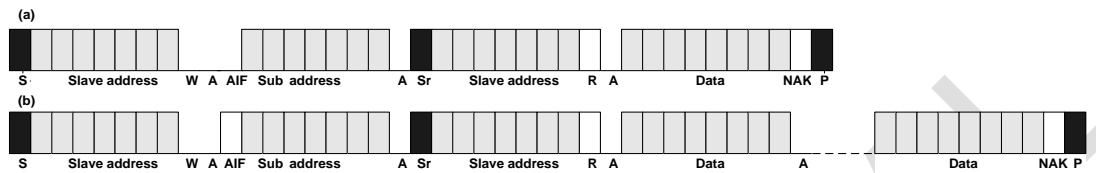
The coefficient mode register address from 0x00 to 0x31 and from 0x5C to 0x65 are used for the Bi-Quad filter coefficients in the coefficient mode. Each Bi-Quad filter uses 5 coefficients. Any unexpected coefficient value changes on any part of 5 coefficients can generate unstable Bi-Quad filter response. For example, if only one of 5 coefficients for a Bi-quad filter is changed and downloaded, its combined 5-coefficient set can have unstable operation while old and new coefficients are mixed together. Therefore to prevent this kind of problem, the NTP8818 writes coefficients to coefficient registers only when the last 5th coefficients of each Bi-quad filter are downloaded, which means all of 5 coefficients are fully ready. Please refer to 9.1 for more detailed operation.

### 5.1.2. Reading Operation

Figure 8-(a) represents single byte reading operation from the NTP8818. To read data from the NTP8818, generate start condition to start transfer. After then, send “slave address” with write mode flag and send the register address(sub address). By regenerating start condition (Sr) again and transferring “slave address” with read mode flag, reading operation begins. The NTP8818 will generate data on SDA signal synchronizing with serial clocks on the SCL. Because the SDA signal generated from the NTP8818, the master device must generate ACK

on 9th slot to confirm that the master received read 1 byte successfully. However, if this is just one byte reading operation, NAK (not acknowledged) signal must be generated. Then stop condition must be generated to end transfer.

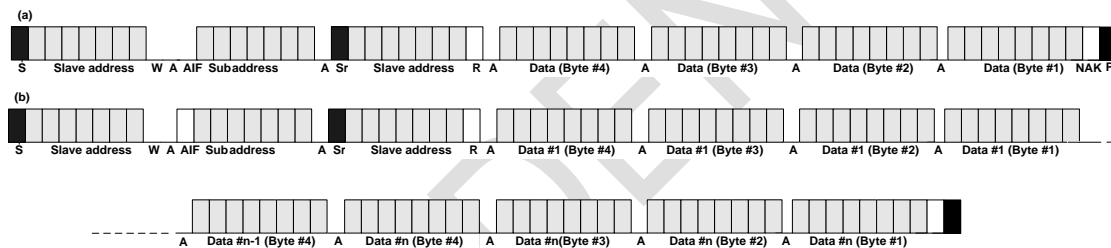
When AIF set to high on sub address like **Figure 8-(b)**, data will be read continuously with register addresses which are increased from initial “sub address” for every byte. To continue reading operation in this case, the master must generate ACK signal on every 9th slot to confirm that master received 1 byte successfully. Otherwise, reading operation will be terminated. To end address auto incrementing reading operation, generate NAK on 9th slot and generate stop condition.



**Figure 8. Single Byte Read Mode Sequence**

**Figure 9** represents quad byte reading operation. The difference between quad byte reading operation and single byte reading operation is only the size of receiving data. So, after sending “Sub address”, 4 sequential bytes must be received from the MSB to the LSB sequence.

The type presented on **Figure 9-(b)** is quad byte read operation under address auto increment mode, AIF function. Please compare the data receive size between **Figure 8** and **Figure 9**.



**Figure 9. Quad Byte Read Mode Sequence**

### 5.1.3. I<sup>2</sup>C Glitch Filter

To clean out the threats of noise in today’s high-speed-board system, the NTP8818 has a glitch elimination filter on the I<sup>2</sup>C ports. Glitches in the transmission lines of the I<sup>2</sup>C port can be safely removed with this function. Please refer to the register 0x66.

### 5.1.4. I<sup>2</sup>C Slave Address

The NTP8818 supports up to four slave address. A master device sends the target slave address on the 1st byte. MSB 7 bits of the 1st byte data are used for the slave address. So, four NTP8818 can be connected to the same MCU at the same time. For multi-chip operation, use the proper I<sup>2</sup>C slave address according to AD pin and the initial state of MONITOR\_1 pin as shown in **Table 2**.

|          |       | MONITOR_1 Pin   |               |                           |
|----------|-------|-----------------|---------------|---------------------------|
| Pin name | Value | Pull-down ('L') | Pull-up ('H') | No pd / pu (default: 'L') |
| AD       | 0     | Addr : 0x54     | Addr : 0x58   | Addr : 0x54               |
|          | 1     | Addr : 0x56     | Addr : 0x5A   | Addr : 0x56               |

**Table 2. I<sup>2</sup>C Slave Address**

## 6. CLOCK, RESET & CONTROL

### 6.1. System Clock

The internal system clock of the NTP8818 is generated from an external master clock by the on-chip PLL. The NTP8818 supports external master clock frequency from 3.072 MHz to 24.576MHz. For proper operation, the registers for the PLL should be set correctly according to master clock frequency (Address 0x02).

### 6.2. Timing Sequence 1 (recommend)

For proper power up, initialization and power down of NTP8818, it is recommend to use the following sequence as shown in **Figure 10**.

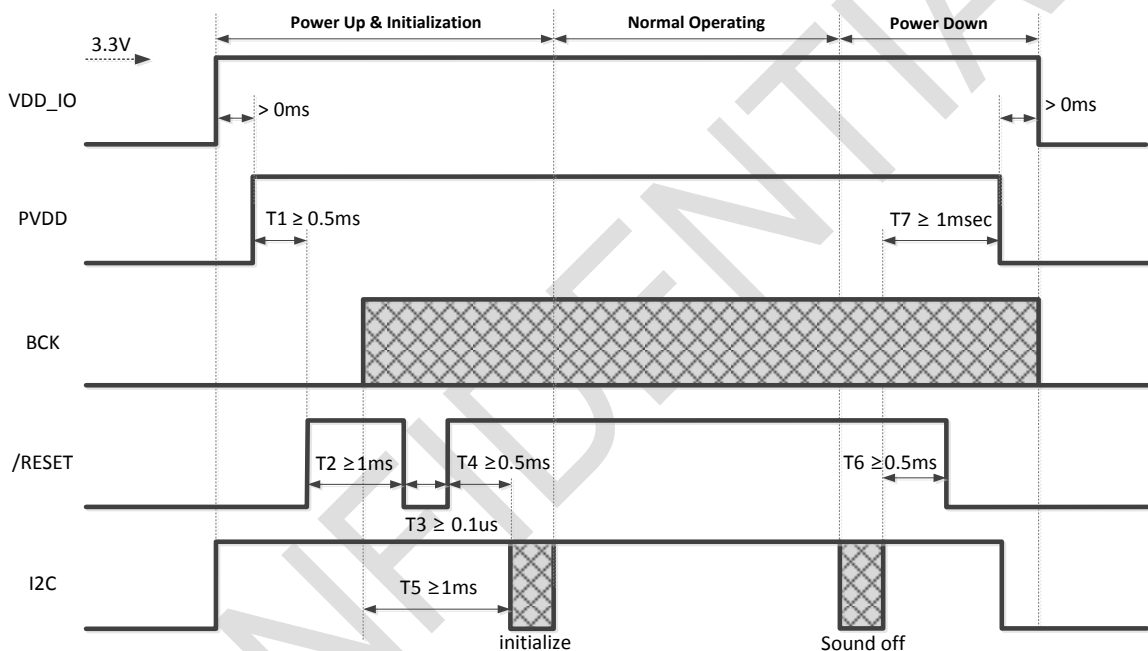


Figure 10. Timing Sequence 1

#### 6.2.1. Power-Up & Initialization Sequence

- 1) Ramp up VDD\_IO to at least 3.3V.
- 2) Ramp up PVDD.
- 3) After 0.5msec ( $T1 \geq 0.5\text{msec}$ ), drive /RESET = High, and then wait for at least 1msec ( $T2 \geq 1\text{msec}$ ).
- 4) Hold /RESET Low for at least 0.1usec ( $T3 \geq 0.1\text{usec}$ )
- 5) Drive /RESET = High, and then wait for at least 0.5msec for I<sup>2</sup>C communication ( $T4 \geq 0.5\text{msec}$ ).
- 6) BCK signal should arrive at least 1msec before I<sup>2</sup>C initialization sequence ( $T5 \geq 1\text{msec}$ ).
- 7) Execute both amp initialization sequence (e.g. clock, volume, DRC, PEQ setup) and Sound on sequence.

#### 6.2.2. Power-Down Sequence

- 1) When both DC and AC power are off, make sure to execute sound off sequence.
- 2) Switch /RESET to Low at least 0.5 msec after sound off sequence ( $T6 \geq 0.5\text{msec}$ ).
- 3) Ramp down PVDD at least 1 msec after sound off sequence ( $T7 \geq 1\text{msec}$ ).
- 4) After I<sup>2</sup>C is Low, ramp down VDD\_IO.

### 6.3. Timing Sequence 2 (reference)

Following figure illustrates another timing sequence, which is conforming to the legacy reset timing.

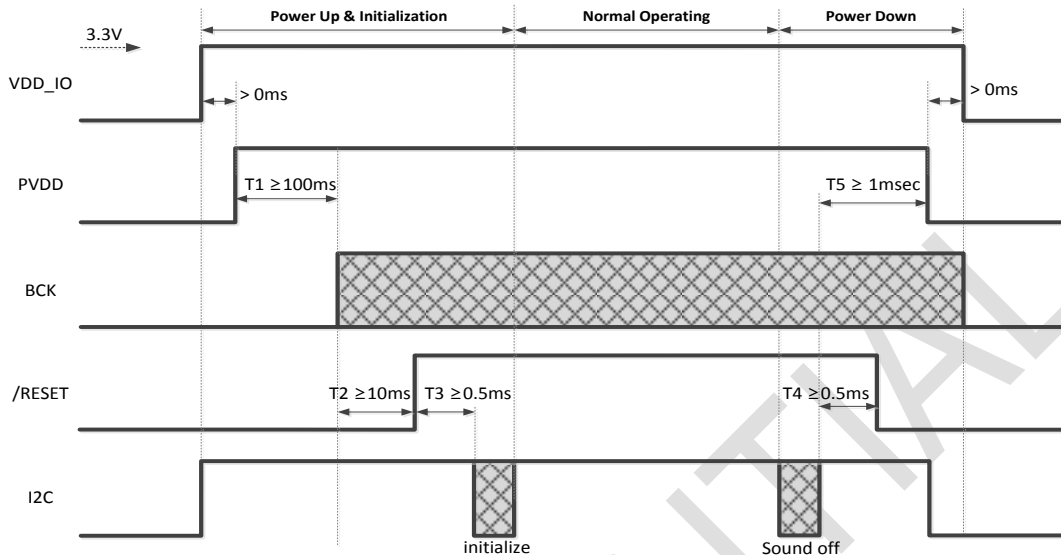


Figure 11. Timing Sequence 2

#### 6.3.1. Power-Up & Initialization Sequence

- 1) Ramp up VDD\_IO to at least 3.3V.
- 2) Ramp up PVDD.
- 3) Drive BCK signal at least 100ms after PVDD ( $T1 \geq 100\text{msec}$ ).
- 4) At least 10ms after BCK, Drive /RESET = High ( $T2 \geq 10\text{msec}$ ).
- 5) Wait for at least 0.5msec for I<sup>2</sup>C communication ( $T3 \geq 0.5\text{msec}$ ) and keep the status.
- 6) Execute both amp initialization sequence (e.g. clock, volume, DRC, PEQ setup) and Sound on sequence.

#### 6.3.2. Power-Down Sequence

- 1) When both DC and AC power are off, make sure to execute sound off sequence.
- 2) Switch /RESET to Low at least 0.5 msec after sound off sequence ( $T4 \geq 0.5\text{msec}$ ).
- 3) Ramp down PVDD at least 1 msec after sound off sequence ( $T5 \geq 1\text{msec}$ ).
- 4) After I<sup>2</sup>C is Low, ramp down VDD\_IO.

### 6.4. Sound On/Off Sequence

For proper sound on/off of NTP8818, use the following sequence as shown in Figure 12.

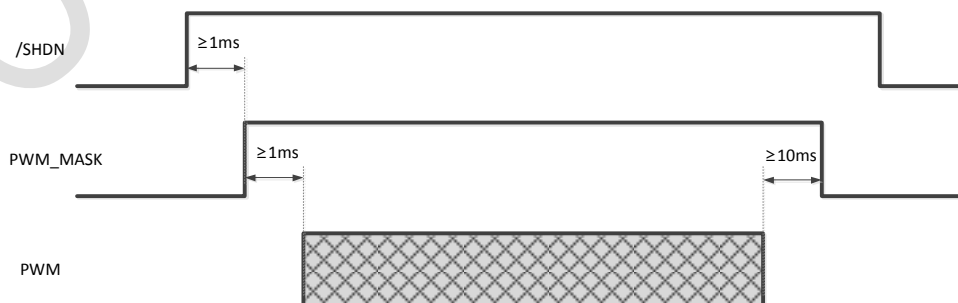


Figure 12. Sound On & Off Sequence

To prevent pop noise when enabling or disabling the amplifier, the following sequences are recommended.

## 7. AUDIO INPUT

### 7.1. I<sup>2</sup>S

NTP8818 receives audio data through digital audio interface. There is a standard digital audio interface - the Inter-IC Sound (I<sup>2</sup>S) Interface.

These interfaces use 2 clock lines and 1 data line to receive the audio data. One of these clock lines is the WCK. A period of the WCK is same with sampling period of audio data i.e. 64bits (32bits for each channel). One of the main function of WCK to define the channels, the low state of WCK indicates the 1<sup>st</sup> channel i.e. left channel and the high state indicate the 2<sup>nd</sup> channel i.e. right channel. This feature enable the clock receiving device to synchronize the data word-wise for transmitting or receiving from clock generating device.

The other clock line is BCK. This clock line used to synchronize the bit-wise data. The number of clock for one WCK period is 64 clock of BCK. The name of data transfer line is SDATA. The data being synchronized with the BCK must be loaded on this line. NTP8818 receive data on rising edge of the BCK. The bit range for I<sup>2</sup>S is predefined.

NTP8818 can only work as a slave on bus. In slave mode, NTP8818 receives WCK and BCK from external source. Please refer the following **Figure 13**.

### 7.2. SDATA Generator

The SDATA generator of NTP8818 sends out I<sup>2</sup>S out signal. In order for SDATA out process to function stably, the falling of BCK should either synchronize or occur ahead of falling or rising of WCK.

Refer to the register Address 0x76 and 0x7C in the **Appendix A** and refer to the **4.6. Switching Characteristics – Audio Interface**.

| SDATA Generator (Sdata out) | Register value             |                            |
|-----------------------------|----------------------------|----------------------------|
|                             | 0x0F                       | 0xF0                       |
| Register Address 0x76       | Sdata out => Monitor 1 pin | Sdata out => Monitor 2 pin |

**Table 3. SDATA Generator Control**

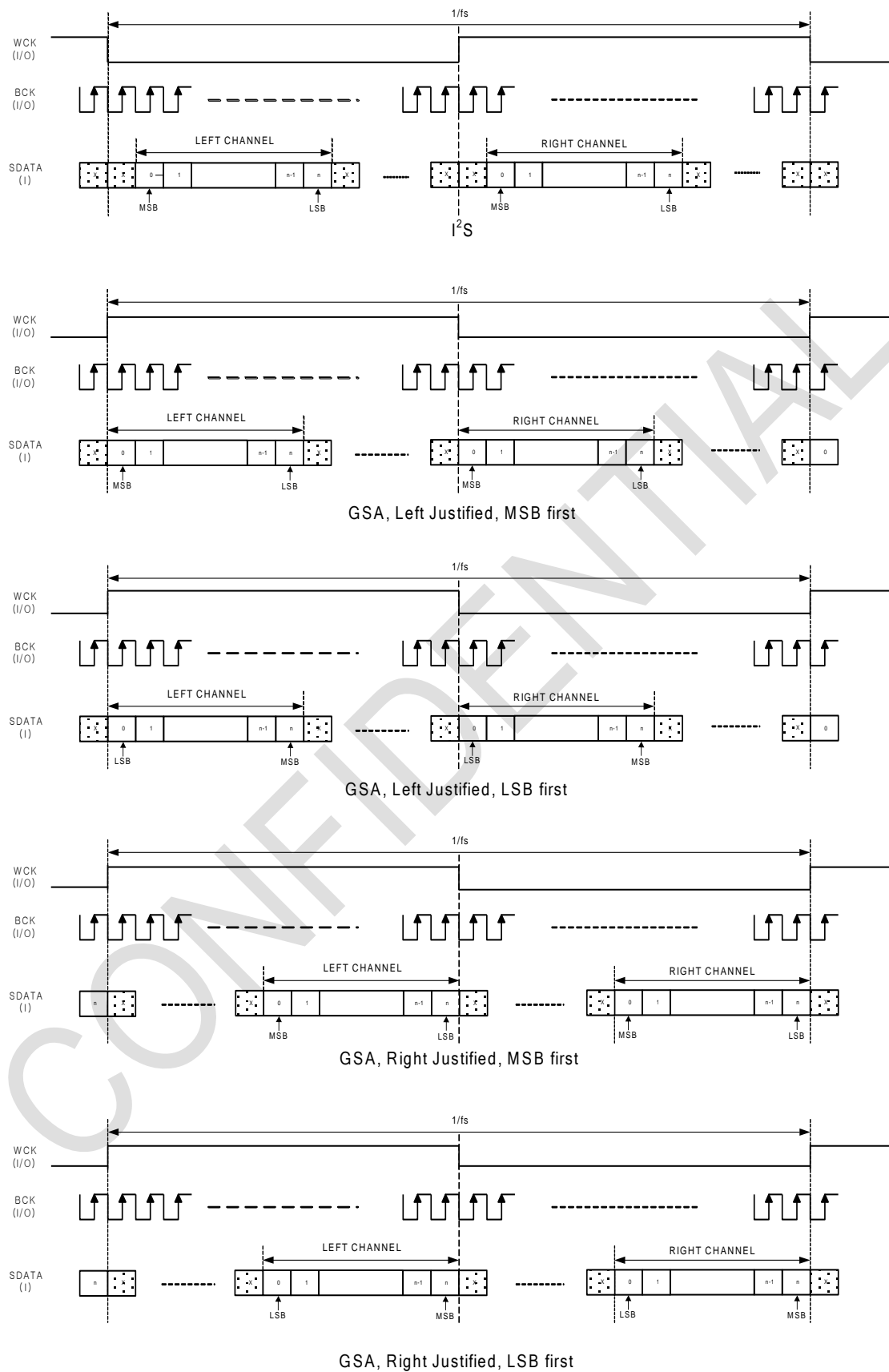


Figure 13. I<sup>2</sup>S Audio Interface Format

## 8. MIXER

Channel mixer can be used in lots of application needs like pseudo stereo and etc. User can mix input channels into each output channels with designated gains and polarity. Step size of mixer gain is variable according to the gain level as shown below.

| Volume Range (dB) | Step (dB) |
|-------------------|-----------|
| +18 ~ +6          | 1         |
| +5.5 ~ -5.5       | 0.5       |
| -6 ~ -32          | 1         |
| ≤ 32              | -∞        |

Table 4. Variable Step Mixing Gain

In total, 4 mixing gain coefficients denoted as M00, M01, M10 and M11 are defined as shown in the equation below. Each Mxx stores volume value in dB scale, and the number values versus gain in dB are shown in the **Appendix B**. By default, each input channel connected to each output channel directly; M00 and M11 are set as 0 dB in plus polarity, M01 and M10 are set as -∞ dB.

$$[\text{Output Channels}] = [\text{Mixer Matrix}] \times [\text{Input Channels}]$$

$$\begin{bmatrix} \text{CH1 OUT} \\ \text{CH2 OUT} \end{bmatrix} = \begin{bmatrix} \text{M00} & \text{M01} \\ \text{M10} & \text{M11} \end{bmatrix} \cdot \begin{bmatrix} \text{CH1 IN} \\ \text{CH2 IN} \end{bmatrix}$$

Figure 14. Serial Mixer Matrix

In order to load mixer coefficients into internal memory, send the index value in the gain value table to the register address 0x03~0x06. Each address matched to M00, M01, M10 and M11 sequentially.

## 9. PRE-PROCESSING

### 9.1. Bi-Quad Filter Chain

The Bi-Quad filter means 2nd order IIR filter. NTP8818 implemented a serial chain of Bi-Quad filters with proprietary floating point operation schemes. The Bi-Quad filter chains can be used in various purposes; loudness control, parametric EQ, loud-speaker EQ, APEQ and etc. The Bi-Quad filter structure is shown in **Figure 15**.

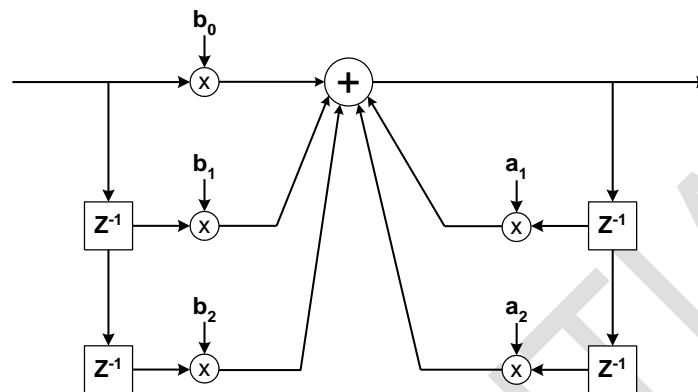


Figure 15. Bi-Quad Filter Structure

Twelve Bi-Quad filters are linked serially for one channel. The Bi-Quad filters can be configured differently for each filter. As shown in **Figure 16**, first three filters can be used for loudness control, last six filters for APEQ control.

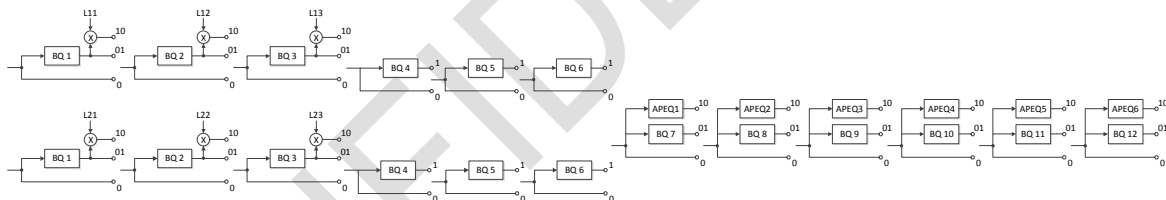


Figure 16. Bi-Quad Filter Chain

Filter coefficients are 32-bit floating point numbers and can be downloaded thru I<sup>2</sup>C interface. To download Bi-Quad filter coefficients to NTP8818, select download channel by using CH flag in register Address 0x7E first. Then, write actual coefficient values to 60 register addresses, from 0x00 to 0x65 in the coefficient register addresses.

The coefficient mode register addresses from 0x00 through 0x04 designate the five coefficients of the first Bi-Quad (BQ1) and represent coefficients b0, b1, b2, a1, a2 respectively. The coefficient mode register addresses from 0x05 through 0x09 designate coefficients of the 2nd Bi-Quad (BQ2) filter, and so on. The enable/disable operation of these Bi-Quad filters can be made by using BQF flag in register addresses of 0x0E~0x15.



| Coefficient Mode register                          | 0x00 ~ 0x04     | 0x05 ~ 0x09     | 0x0A ~ 0x0E     | 0x0F ~ 0x13     | 0x14 ~ 0x18      | 0x19 ~ 0x1D     |             |
|--|-----------------|-----------------|-----------------|-----------------|------------------|-----------------|-------------|
| When system address<br>0x7E = 0x01,<br>0x7E = 0x02 | BQ1 of<br>CH1/2 | BQ2 of<br>CH1/2 | BQ3 of<br>CH1/2 | BQ4 of<br>CH1/2 | BQ5 of<br>CH1/2  | BQ6 of<br>CH1/2 |             |
| Coefficient Mode register                          | 0x1E ~ 0x22     | 0x23 ~ 0x27     | 0x28 ~ 0x2C     | 0x2D ~ 0x31     | 0x50 ~ 0x52      | 0x5C ~ 0x60     | 0x61 ~ 0x65 |
| When system address<br>0x7E = 0x01                 | BQ7             | BQ8             | BQ9             | BQ10            | Loudness<br>Gain | BQ11            | BQ12        |

| Coefficient Mode register          | 0x00 ~ 0x05                    | 0x06 ~ 0x0B                    | 0x0C ~ 0x011                   | 0x12 ~ 0x17                    | 0x1F ~ 0x24                       |
|------------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|-----------------------------------|
| When system address<br>0x7E = 0x08 | Coefficient 0 of<br>APEQ 1 ~ 6 | Coefficient 1 of<br>APEQ 1 ~ 6 | Coefficient 2 of<br>APEQ 1 ~ 6 | Coefficient 3 of<br>APEQ 1 ~ 6 | Coefficient 4<br>of APEQ 1 ~<br>6 |

**Table 5. Address of Coefficients for Bi-Quad Filter Chain**

### 9.2. Loudness Control

NTP8818 provides loudness control function using coefficient values. Loudness control means the compensation of frequency characteristics in low volume level to fit the acoustic characteristics of human ears.

There are 3 coefficient values for loudness gain per each channel. To download a loudness gain of each coefficient, the page flag register 0x7E should be set as same in the case of downloading the filter coefficients. The loudness gain values are applied for both channel 1 and 2, and when downloading the loudness gain values, a user should set the register 0x7E as 0x03.

| loudness gains of CH1/CH2        | Coefficient Mode Register Address |      |      |
|----------------------------------|-----------------------------------|------|------|
|                                  | 0x50                              | 0x51 | 0x52 |
| Register Address 0x7E= 0x03 case | L1                                | L2   | L3   |

**Table 6. Address for Loudness Gain**

### 9.3. Advanced Parametric Equalizer

NTP8818 has a new scheme for APEQ function using coefficient values. APEQ function means the compensation of frequency characteristics based on input signal level to fit the acoustic characteristics of human ears.

APEQ needs a Bi-Quad filter coefficient and five additional coefficients, which comprise a gain coefficient and a threshold coefficient. To download each coefficient, the page flag register 0x7E should be set as same in the case of downloading the filter coefficients. The coefficient values are applied for both channel 1 and 2.

| APEQ coefficient of<br>CH1/CH2       | Coefficient mode register address |                          |                          |                          |                               |
|--------------------------------------|-----------------------------------|--------------------------|--------------------------|--------------------------|-------------------------------|
|                                      | 0x00 ~ 0x05                       | 0x06 ~ 0x0B              | 0x0C ~ 0x11              | 0x12 ~ 0x17              | 0x1F ~ 0x24                   |
| Register Address<br>0x7E = 0x08 case | Coefficient 0<br>f(Gain)          | Coefficient 1<br>f(Gain) | Coefficient 2<br>f(Gain) | Coefficient 3<br>f(Gain) | Coefficient 4<br>f(Threshold) |

**Table 7. Address for APEQ Coefficient**

## 10. VOLUME & DYNAMIC RANGE CONTROL

Master and channel volumes of the NTP8818 are independently controlled and softly changed. The system register address 0x0C is the master volume control that affects both channels simultaneously and the address 0x17 and 0x18 correspond to the channel volume control register for channel 1 and 2 respectively.

The possible Maximum Gain is +48.375dB with using master volume fine control, master volume and channel volume because the master volume applies the gain to an input signal independent from a channel volume. However, in such a case, a clipping might occur to prevent a signal overflow error if the magnitude of the input signal is large enough to exceed 0dB under the combined volume setting.

### 10.1. Master Volume Control

By setting volume control register (address 0x0C), master volume is controlled from negative infinity through 0dB with selectable step size as follows. For details on the master volume setting, see the register value table shown in **Appendix B**.

| Step   | Range       |
|--------|-------------|
| 0.5 dB | 0 ~ -125 dB |

Table 8. Level Dependent Master Volume Steps

### 10.2. Channel Volume Control

By setting volume control registers (address 0x17 and 0x18), channel volumes are independently controlled from negative infinity through +48dB with two selectable step sizes as described below, and in the **Appendix B**, exact values for channel volume setting are described.

| Step   | Range        |
|--------|--------------|
| 0.5 dB | +48 ~ -79 dB |

Table 9. Level Dependent Channel Volume Steps

### 10.3. Master Volume Fine Control

Fine control for master volume is possible (+0.125dB step up to maximum +0.375dB boost). Refer the system register Address 0x16 in the **Appendix A**.

### 10.4. Mute and Soft Volume Change

The NTP8818 enters mute state by setting soft mute flag of register Address 0x33. Soft mute is implemented so that the volume gradually increases or decreases when mute is turned off or on respectively. Also the soft mute speed and soft volume change speed rates are programmable. Designers can minimize the pop noise by controlling the soft mute speed and volume change intervals. Refer SM flag of register Address 0x33 and SVI flag of register Address 0x30.

### 10.5. Auto Mute

The NTP8818 can mute the sound automatically when the level of input audio signal is lower than the register-controlled threshold value. The mute can be done by PWM switching with 50 % duty ratio.

Auto mute is supported for internal channels 1~2 after 2x2 mixer block. Refer register Address 0x3A.

### 10.6. Dynamic Range Control

NTP8818 has a new scheme for dynamic range control, which comprise a high band DRC, a low band DRC, a sub band DRC and a post DRC. The input data is filtered by HPF, LPF and SPF, and then processed by H-DRC, L-DRC and SDRC respectively. Three processed results are merged and followed by post DRC, which produces the output data with the fully controlled dynamic range. For detailed setting of the DRC registers, please refer to the system register addresses in Table 10.

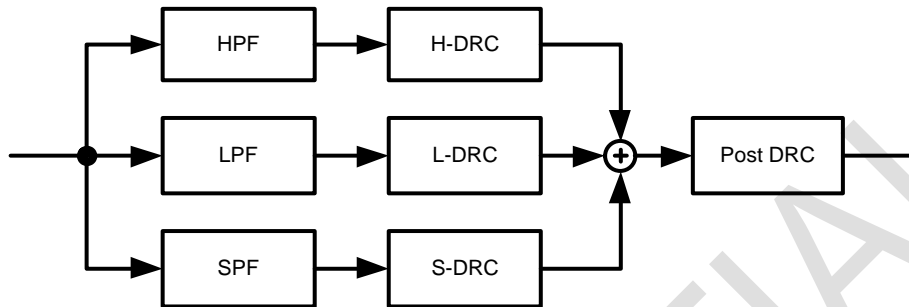


Figure 17. Block Diagram of Dynamic Range Control

|                                   |               |               |               |               |               |               |
|-----------------------------------|---------------|---------------|---------------|---------------|---------------|---------------|
| 3B' DRC Coefficient mode register | 0x32 ~ 0x36   | 0x37 ~ 0x3B   | 0x3C ~ 0x40   | 0x41 ~ 0x45   | 0x46 ~ 0x4A   | 0x4B ~ 0x4F   |
| When System Address 0x7E = 0x03   | LPF1 of L-DRC | LPF2 of L-DRC | HPF1 of H-DRC | HPF2 of H-DRC | SPF1 of S-DRC | SPF2 of S-DRC |

Table 10. Coefficient Register Map for Dynamic Range Control

### 10.7. Power Meter

The power meter measures signal's energy of internal, send value of energy through register address 0x2E and always operates without on/off control, and read value through register address 0x2F.

(refer to the **Table 20. Power Meter Reading Table**)

Because audio signals swing very rapidly in process of time, a user can use the power meter gain to get stable value of energy. The more power meter gain approaches to maximum value, the more value of energy changes slowly.

Power meter gain is 32-bit floating point numbers and can be downloaded thru I<sup>2</sup>C interface. To download power meter gain, page flag register 0x7E should be set 0x01 or 0x03. And then write gain value to 0x58 register address.

## 11. OUTPUT INTERFACE

### 11.1. Output Configuration

The output of NTP8818 has various options. To produce proper output signal, register 0x3C, 0x34, 0x3E, 0x3F, 0x40 and 0x43 should be set to appropriate values.

### 11.2. PWM Output Mapper

Any internal channel that produces a PWM output can be assigned to any PWM output hardware port (or pin) by mapping output port register. This feature is very helpful for the hardware designer because it can relieve difficulties in the power stage signal routing and channel assignment if the output channel order is fixed. See the system register address 0x40 in the **Appendix A**.

### 11.3. Switching Output Mode

There are two selectable switching output modes in NTP8818. The difference between two output modes lies in the relationship of the relative signal pattern between PWM OUTxA and PWM OUTxB for a channel x. The first one is called as AD mode. This AD mode can be applied to both half bridge and full bridge output stage.

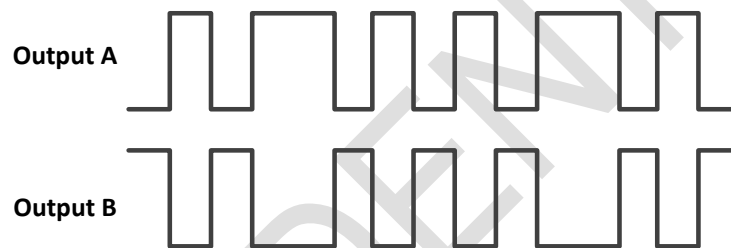


Figure 18. PWM Output Signals in AD Mode

AD asynchronous pair means the normal AD mode PWM output. In other words, A output and B output of each PWM output pair are mutually complementary. In the case of AD synchronous pair, A output and B output is perfectly identical, and its relation is not complementary. This is useful in some special case including single-ended power stage design.

The other one is called as NTX (Neo Trinity Amplification), which is D-BTL mode. This mode is applied only for BTL, and its operation is dynamically-biased BTL, compared to the normal BTL. An example of output signals in D-BTL mode is shown in **Figure 19**.

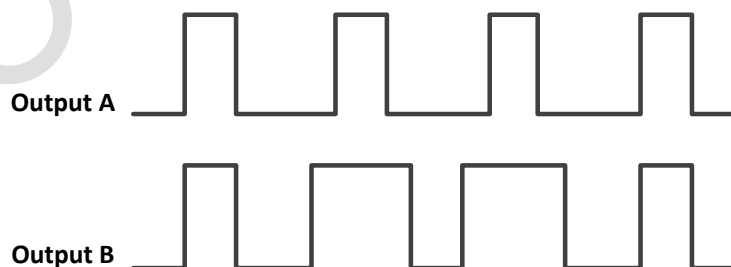
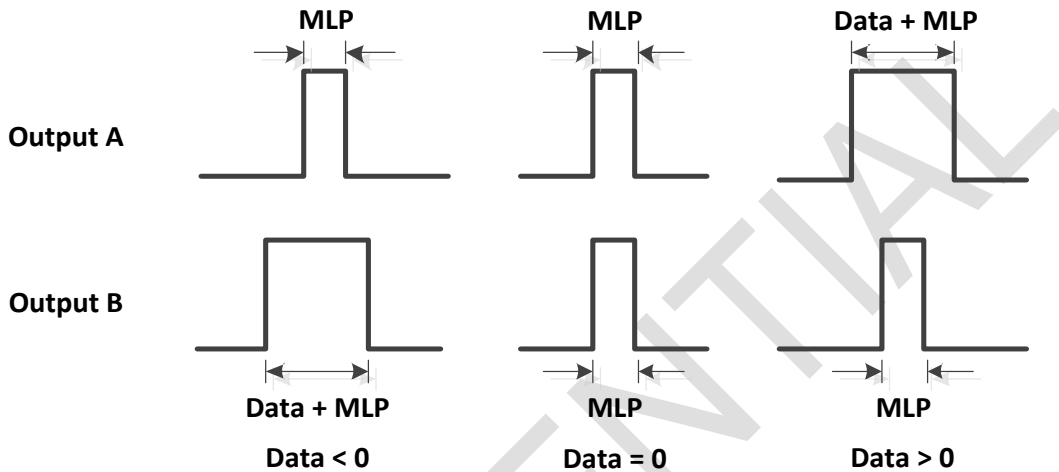


Figure 19. PWM Output Signals in D-BTL Mode

For D-BTL mode, there are two additional parameters, which is MLP (Minimum Linear Pulse Length). MLP defines the minimum pulse length that can guarantee a linear relationship between the input and output pulse length. Generally, the width of the output pulse is proportional to that of the input pulse. However, as the width of input pulse becomes narrower, such linear relation is not maintained due to the characteristic of a power device. The minimum MLP value is preferred as long as linear relationship between the input and the output pulse is satisfied. In addition, in terms of power consumption, a minimal MLP value is preferred.

This compensation is illustrated in **Figure 20**.

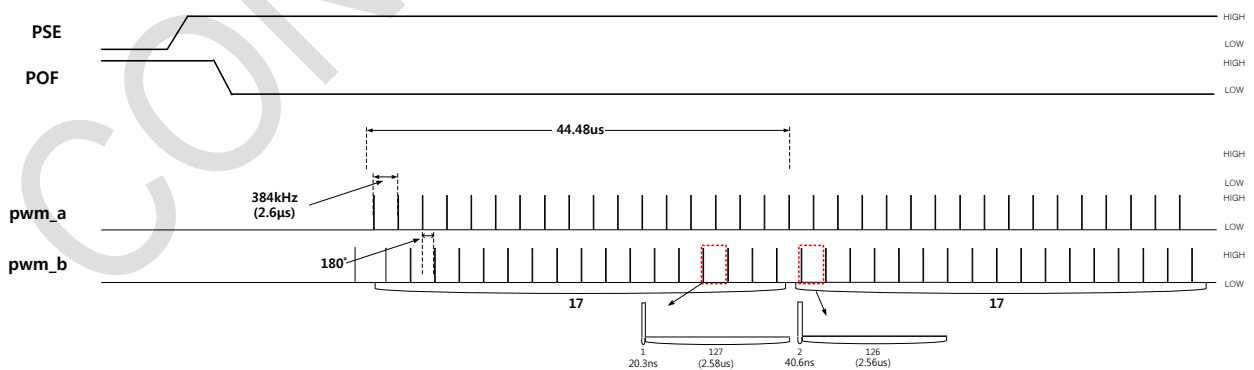


**Figure 20. Compensation by MLP**

#### 11.4. Soft Start

The soft\_start reduces pop noise by controlling rapidly increased energy of PWM.

To begin soft\_start operation, PWM soft start enable register (0x4A: PSE) should be set to high, and then PWM switching on/off register (0x34: POF) should be set to low. The duty ratio of PWM output increases from 127:1 (Low:High) to 50:50 (Low:High). Step repeat time register (0x4A: SRT) means repeat number of PWM output in one duty sector. Soft\_start operation with 17 repetitions is shown in the **Figure 21**.



**Figure 21. Soft Start Operation Timing**

## 12. DC PROTECTION

This DC protection block prevents the system from outputting DC signal, which can cause a speaker unit burnt. Three sub functions are employed to prevent DC output, which are monitoring a memory checksum, observing a modulation index, and cutting DC output via hard-wired filters. Except for the hard-wired DC cut filter, the other two blocks only reports the error status, and external MCU may reset the amplifier chip by setting the DC soft reset register to high.

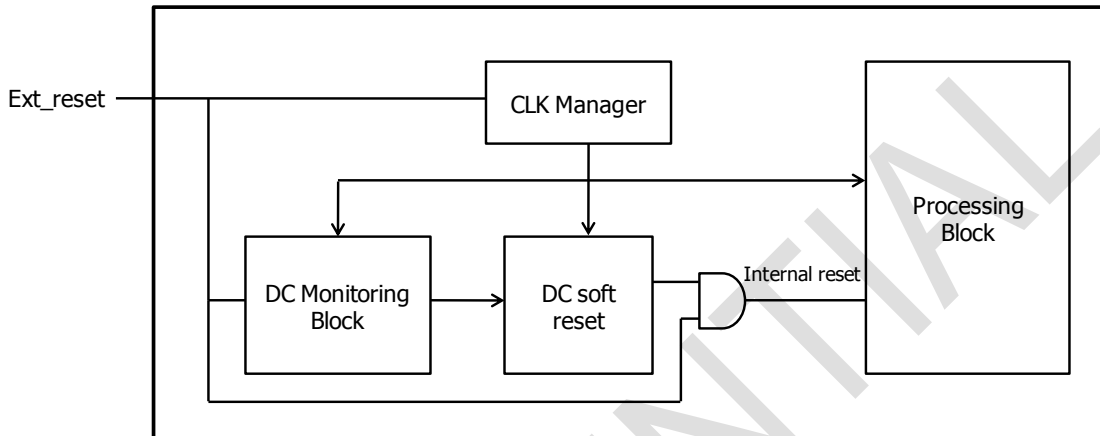


Figure 22. Block Diagram for DC PROTECTION

### 12.1 Memory Checksum

While initializing the system, the checksum data of coefficients are downloaded from the external MCU from the address 0x53 through 0x5A. This memory checksum block compares the checksum data of current memory block and the checksum data at the initial time. If there happens a discrepancy between two values due to some memory fault, the error flag of address 0x5B is set to high. The external MCU can monitor this error flag and reset the chip by setting the DC soft reset to high at address 0x52. This DC soft reset will initialize the whole chip, and initialization process of the memory should be done thereafter.

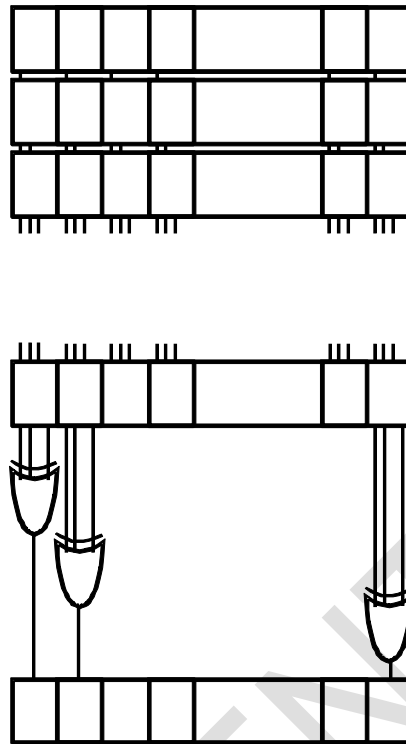


Figure 23. Structure of Memory Checksum

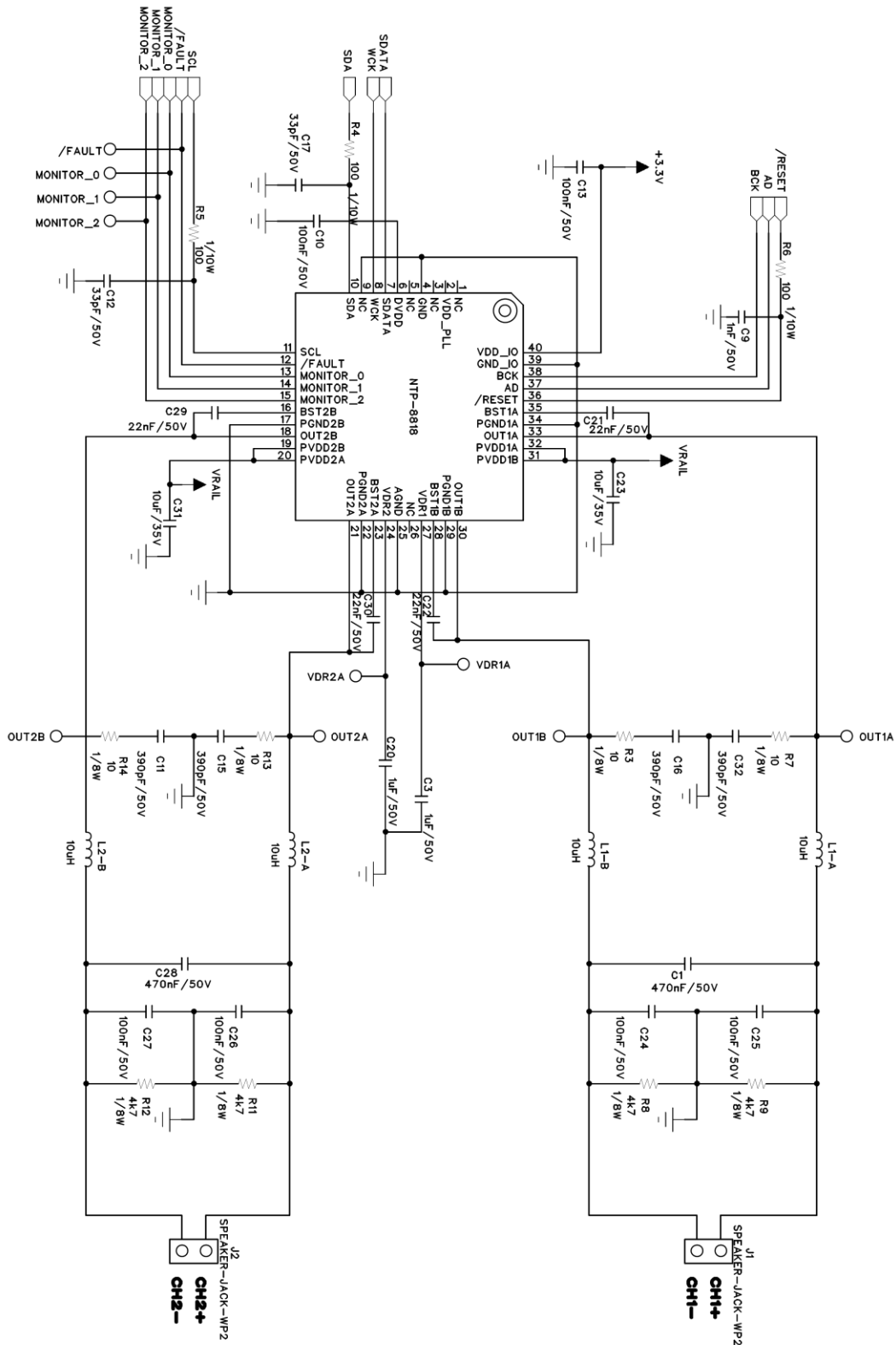
### 12.2 Modulation Index Check

When there is a DC component in the output, the modulation index tends to stay over or under certain value. The modulation index check block constantly monitors the PWM modulation index, and if the index value continues to stay over or under certain period of time, it sets modulation index error flag of address 0x5B to high. The external MCU can monitor this error flag and reset the chip by setting the DC soft reset the register value of address 0x52 to high. The PWM modulation duty at address 0x50 and 0x51 can be set to decide the level of DC monitoring for AD and D-BTL mode respectively.

### 12.3 Hard-wired DC cut

The hard-wired DC cut filters prevent the system from outputting the signal of less than 1Hz frequency. The hard-wired DC cut filters exist in the Bi-quad filter chain.

### 13. TYPICAL APPLICATION SCHEMATICS





## 14. APPENDIX

### A. Configuration Register Summary

#### Addr 0x00: Audio Input Format

|      |   |   |   |   |   |   |   |     |
|------|---|---|---|---|---|---|---|-----|
| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0   |
| Name | X | X | X | X | X | X | X | INS |

| Name | Description  | Value | Meaning                          | Ref. |
|------|--------------|-------|----------------------------------|------|
| INS  | Input format | b'0   | I <sup>2</sup> S, slave mode     |      |
|      |              | b'1   | General serial audio, slave mode |      |

#### Addr 0x01: General Serial Audio Format

|      |   |   |      |   |    |   |     |     |
|------|---|---|------|---|----|---|-----|-----|
| Bit  | 7 | 6 | 5    | 4 | 3  | 2 | 1   | 0   |
| Name | X | X | BCKS |   | BS |   | MLF | LRJ |

| Name | Description           | Value | Meaning       | Ref. |
|------|-----------------------|-------|---------------|------|
| LRJ  | Serial data justify   | b'0   | Left justify  |      |
|      |                       | b'1   | Right justify |      |
| MLF  | Serial bit order      | b'0   | MSB first     |      |
|      |                       | b'1   | LSB first     |      |
| BS   | Serial bit size       | b'00  | 24 bit        |      |
|      |                       | b'01  | 20 bit        |      |
|      |                       | b'10  | 18 bit        |      |
|      |                       | b'11  | 16 bit        |      |
| BCKS | Bit clock size select | b'00  | 64 BCK/WCK    |      |
|      |                       | b'01  | 48 BCK/WCK    |      |
|      |                       | b'10  | 32 BCK/WCK    |      |

#### Addr 0x02: Master Clock Frequency Control

|      |   |   |   |   |   |     |   |   |
|------|---|---|---|---|---|-----|---|---|
| Bit  | 7 | 6 | 5 | 4 | 3 | 2   | 1 | 0 |
| Name | X | X | X | X | X | MCF |   |   |

| Name | Description            | Value | Meaning  | Ref. |
|------|------------------------|-------|--|------|
| MCF  | Master Clock Frequency | b'000 | 3.072 MHz (WCK 48 kHz) / 2.8224 MHz (WCK 44.1 kHz) |      |
|      |                        | b'001 | 6.144 MHz (WCK 96 kHz)                             |      |
|      |                        | b'010 | 2.048 MHz (WCK 32 kHz)                             |      |
|      |                        |       |  |      |

#### Addr 0x03~0x06: Mixer Gain

|      |   |    |   |   |   |   |   |   |
|------|---|----|---|---|---|---|---|---|
| Bit  | 7 | 6  | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | X | MG |   |   |   |   |   |   |

| Name | Description | Value       | Meaning                          | Ref. |
|------|-------------|-------------|----------------------------------|------|
| MG   | Mixer gain  | h'00 ~ h'7E | Mixer gain (refer to gain table) |      |

$$\begin{bmatrix} mixer\_ch1\_output \\ mixer\_ch2\_output \end{bmatrix} = \begin{bmatrix} 0x03 & 0x04 \\ 0x05 & 0x06 \end{bmatrix} \cdot \begin{bmatrix} I2S\_ch1\_input \\ I2S\_ch2\_input \end{bmatrix}$$

Mixer equation

$$\begin{bmatrix} mixer\_ch1\_output \\ mixer\_ch2\_output \end{bmatrix} = \begin{bmatrix} 0dB(0x4E) & -\infty dB(0x00) \\ -\infty dB(0x00) & 0dB(0x4E) \end{bmatrix} \cdot \begin{bmatrix} I2S\_ch1\_input \\ I2S\_ch2\_input \end{bmatrix}$$

Reset default

**Reserved Address 0x08 ~ 0x0B**

**Addr 0x0C: Master Volume & SPK PWM Switching On/Off Control**

|      |      |   |   |   |   |   |      |   |
|------|------|---|---|---|---|---|------|---|
| Bit  | 7    | 6 | 5 | 4 | 3 | 2 | 1    | 0 |
| Name | MVOL |   |   |   |   |   | SPOF |   |

| Name | Description                           | Value                   | Meaning   | Ref. |
|------|---------------------------------------|-------------------------|---|------|
| SPOF | Smart Switching Output on/off Control | b'00000000              | PWM off<br>(softmute on → pwm off → pwm_mask low)   |      |
|      |                                       | b'00000001              | PWM off<br>(softmute on → pwm off → pwm_mask high)  |      |
|      |                                       | b'00000010              | PWM on<br>(softmute on → pwm_mask high → pwm on)  |      |
|      |                                       | b'00000011              | PWM on<br>(pwm_mask high → pwm on → softmute off)   |      |
| MVOL | Volume control                        | b'00000100 ~ b'11111111 | refer to master volume table. Reset default is 0x00 (= -∞ dB). 0xFF means 0dB with 0.5dB step |      |

**Reserved Address 0x0D**

**Addr 0x0E~0x0F: PEQ Filter Control 0 for Ch1 and Ch2 respectively**

|      |   |   |     |   |     |   |     |   |
|------|---|---|-----|---|-----|---|-----|---|
| Bit  | 7 | 6 | 5   | 4 | 3   | 2 | 1   | 0 |
| Name | X | X | BQ3 |   | BQ2 |   | BQ1 |   |

| Name | Description                        | Value | Meaning                             | Ref. |
|------|------------------------------------|-------|-------------------------------------|------|
| BQ1  | On/off Bi-Quad 1 of ch. n (n= 1,2) | b'00  | Bypass Bi-Quad 1 of channel n       |      |
|      |                                    | b'01  | Enable Bi-Quad 1 of channel n       |      |
|      |                                    | b'10  | Enable Bi-Quad 1 as Loudness Filter |      |
| BQ2  | On/off Bi-Quad 2 of ch. n (n= 1,2) | b'00  | Bypass Bi-Quad 2 of channel n       |      |
|      |                                    | b'01  | Enable Bi-Quad 2 of channel n       |      |
|      |                                    | b'10  | Enable Bi-Quad 2 as Loudness Filter |      |
| BQ3  | On/off Bi-Quad 3 of ch. n (n= 1,2) | b'00  | Bypass Bi-Quad 3 of channel n       |      |
|      |                                    | b'01  | Enable Bi-Quad 3 of channel n       |      |
|      |                                    | b'10  | Enable Bi-Quad 3 as Loudness Filter |      |

**Addr 0x10~0x11: PEQ Filter Control 1 for Ch1, Ch2 respectively**

|      |   |   |   |   |   |     |     |     |
|------|---|---|---|---|---|-----|-----|-----|
| Bit  | 7 | 6 | 5 | 4 | 3 | 2   | 1   | 0   |
| Name | X | X | X | X | X | BQ6 | BQ5 | BQ4 |

| Name | Description                         | Value | Meaning                       | Ref. |
|------|-------------------------------------|-------|-------------------------------|------|
| BQ4  | On/off Bi-Quad 4 of ch. n (n= 1,2)  | b'0   | Bypass Bi-Quad 4 of channel n |      |
|      |                                     | b'1   | Enable Bi-Quad 4 of channel n |      |
| BQ5  | On/off Bi-Quad 5 of ch. n (n = 1,2) | b'0   | Bypass Bi-Quad 5 of channel n |      |
|      |                                     | b'1   | Enable Bi-Quad 5 of channel n |      |
| BQ6  | On/off Bi-Quad 6 of ch. n (n = 1,2) | b'0   | Bypass Bi-Quad 6 of channel n |      |
|      |                                     | b'1   | Enable Bi-Quad 6 of channel n |      |

**Addr 0x12~0x13: APEQ Filter Control 0 for Ch1 and Ch2 respectively**

|      |      |   |     |   |     |   |     |   |
|------|------|---|-----|---|-----|---|-----|---|
| Bit  | 7    | 6 | 5   | 4 | 3   | 2 | 1   | 0 |
| Name | BQ10 |   | BQ9 |   | BQ8 |   | BQ7 |   |

| Name | Description                          | Value       | Meaning                                | Ref. |
|------|--------------------------------------|-------------|--|------|
| BQ7  | On/off Bi-Quad 7 of ch. n (n = 1,2)  | <b>b'00</b> | Bypass Bi-Quad 7 of channel n          |      |
|      |                                      | b'01        | Enable Bi-Quad 7 of channel n          |      |
|      |                                      | b'10        | Enable Bi-Quad 7 of channel n as APEQ  |      |
|      |                                      | b'11        | Reserved                               |      |
| BQ8  | On/off Bi-Quad 8 of ch. n (n = 1,2)  | <b>b'00</b> | Bypass Bi-Quad 8 of channel n          |      |
|      |                                      | b'01        | Enable Bi-Quad 8 of channel n          |      |
|      |                                      | b'10        | Enable Bi-Quad 8 of channel n as APEQ  |      |
|      |                                      | b'11        | Reserved                               |      |
| BQ9  | On/off Bi-Quad 9 of ch. n (n = 1,2)  | <b>b'00</b> | Bypass Bi-Quad 9 of channel n          |      |
|      |                                      | b'01        | Enable Bi-Quad 9 of channel n          |      |
|      |                                      | b'10        | Enable Bi-Quad 9 of channel n as APEQ  |      |
|      |                                      | b'11        | Reserved                               |      |
| BQ10 | On/off Bi-Quad 10 of ch. n (n = 1,2) | <b>b'00</b> | Bypass Bi-Quad 10 of channel n         |      |
|      |                                      | b'01        | Enable Bi-Quad 10 of channel n         |      |
|      |                                      | b'10        | Enable Bi-Quad 10 of channel n as APEQ |      |
|      |                                      | b'11        | Reserved                               |      |

**Addr 0x14~0x15: APEQ Filter Control 1 for Ch1 and Ch2 respectively**

|      |   |   |   |   |      |   |      |   |
|------|---|---|---|---|------|---|------|---|
| Bit  | 7 | 6 | 5 | 4 | 3    | 2 | 1    | 0 |
| Name | X | X | X | X | BQ12 |   | BQ11 |   |

| Name | Description                          | Value       | Meaning                                | Ref. |
|------|--------------------------------------|-------------|--|------|
| BQ11 | On/off Bi-Quad 11 of ch. n (n = 1,2) | <b>b'00</b> | Bypass Bi-Quad 11 of channel n         |      |
|      |                                      | b'01        | Enable Bi-Quad 11 of channel n         |      |
|      |                                      | b'10        | Enable Bi-Quad 11 of channel n as APEQ |      |
|      |                                      | b'11        | Reserved                               |      |
| BQ12 | On/off Bi-Quad 12 of ch. n (n = 1,2) | <b>b'00</b> | Bypass Bi-Quad 12 of channel n         |      |
|      |                                      | b'01        | Enable Bi-Quad 12 of channel n         |      |
|      |                                      | b'10        | Enable Bi-Quad 12 of channel n as APEQ |      |
|      |                                      | b'11        | Reserved                               |      |

**Addr 0x16: Master Volume Fine Control**

|      |   |   |   |   |   |   |      |   |
|------|---|---|---|---|---|---|------|---|
| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0 |
| Name | X | X | X | X | X | X | MVFC |   |

| Name | Description                | Value                 | Meaning                            | Ref. |
|------|----------------------------|-----------------------|------------------------------------|------|
| MVFC | Master volume fine control | <b>b'00</b> ~<br>b'11 | 0 dB ~ 0.375 dB with 0.125 dB step |      |

**Addr 0x17~0x18: Ch1/2 Volume, respectively**

|      |     |   |   |   |   |   |   |   |
|------|-----|---|---|---|---|---|---|---|
| Bit  | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | VOL |   |   |   |   |   |   |   |

| Name | Description    | Value                      | Meaning   | Ref. |
|------|----------------|----------------------------|---|------|
| VOL  | Volume control | b'00000000 ~<br>b'11111111 | refer to channel volume table.<br>Reset default is <b>0x9F</b> (= 0dB).<br>0xFF means 48dB with 0.5dB step. |      |

**Addr 0x19: APEQ Path Option**

|      |   |   |   |   |   |     |   |   |
|------|---|---|---|---|---|-----|---|---|
| Bit  | 7 | 6 | 5 | 4 | 3 | 2   | 1 | 0 |
| Name | X | X | X | X | X | OPT |   |   |

| Name | Description      | Value | Meaning                           | Ref.   |
|------|------------------|-------|-----------------------------------|--|
| Opt  | APEQ Path Option | b'000 | cut1=>Vol=>PEQ6=>APEQ6=>DRC=>cut2 | Set b'000 for APEQ op. (Same effect btw b'000 & b'010) |
|      |                  | b'001 | Reserved                          |  |
|      |                  | b'010 | cut1=>PEQ6=>Vol=>APEQ6=>DRC=>cut2 |  |
|      |                  | b'011 | Reserved                          |  |
|      |                  | b'100 | cut1=>PEQ6=>APEQ6=>Vol=>DRC=>cut2 |  |
|      |                  | b'101 | Reserved                          |  |

**Addr 0x1A: APEQ Filter Control 2 for APEQ1 (BQ7)**

|      |   |         |   |   |         |   |   |   |
|------|---|---------|---|---|---------|---|---|---|
| Bit  | 7 | 6       | 5 | 4 | 3       | 2 | 1 | 0 |
| Name | X | C1C_DP1 |   |   | A1C_DP1 |   |   |   |

| Name    | Description       | Value            | Meaning   | Ref. |
|---------|-------------------|------------------|---|------|
| A1C_DP1 | APEQ attack time  | b'0000<br>b'1010 | ~ Attack time control (refer to APEQ attack time table below)   |      |
| C1C_DP1 | APEQ release time | b'000<br>b'111   | ~ Release time control (refer to APEQ release time table below) |      |

| Value of Register | Attack time 6dB, fs = 96,000 |
|-------------------|------------------------------|
| 0011              | 15msec                       |
| 0010              | 8msec                        |
| 0001              | 4msec                        |
| 0000              | 2msec                        |
| 0111              | 1msec                        |
| 0110              | 0.5msec                      |
| 0101              | 0.25msec                     |
| 0100              | 0.125msec                    |
| 1000              | 2.5msec                      |
| 1001              | 3msec                        |
| 1010              | 3.5msec                      |

**Table 11. APEQ Attack Time Table**

| Value of Register | Release time 6dB, fs = 96,000 |
|-------------------|-------------------------------|
| 011               | 5.0sec                        |
| 010               | 2.0sec                        |
| 001               | 1.0sec                        |
| 000               | 0.5sec                        |
| 111               | 0.2sec                        |
| 110               | 0.1sec                        |
| 101               | 0.05sec                       |
| 100               | 0.025sec                      |

**Table 12. APEQ Release Time Table**

**Addr 0x1B: APEQ Filter Control 3 for APEQ2 (BQ8)**

|      |   |         |   |   |         |   |   |   |
|------|---|---------|---|---|---------|---|---|---|
| Bit  | 7 | 6       | 5 | 4 | 3       | 2 | 1 | 0 |
| Name | X | C1C_DP2 |   |   | A1C_DP2 |   |   |   |

| Name    | Description       | Value            | Meaning  | Ref. |
|---------|-------------------|------------------|--|------|
| A1C_DP2 | APEQ attack time  | b'0000<br>b'1010 | ~ Attack time control (refer to APEQ attack time table in Addr 0x1A)   |      |
|         |                   |                  |  |      |
| C1C_DP2 | APEQ release time | b'000<br>b'111   | ~ Release time control (refer to APEQ release time table in Addr 0x1A) |      |
|         |                   |                  |  |      |

**Addr 0x1C: APEQ Filter Control 4 for APEQ3 (BQ9)**

|      |   |         |   |   |         |   |   |   |
|------|---|---------|---|---|---------|---|---|---|
| Bit  | 7 | 6       | 5 | 4 | 3       | 2 | 1 | 0 |
| Name | X | C1C_DP3 |   |   | A1C_DP3 |   |   |   |

| Name    | Description       | Value                   | Meaning   | Ref. |
|---------|-------------------|-------------------------|---|------|
| A1C_DP3 | APEQ attack time  | <b>b'0000</b><br>b'1010 | ~ Attack time control<br>(refer to APEQ attack time table in Addr 0x1A)   |      |
| C1C_DP3 | APEQ release time | <b>b'000</b><br>b'111   | ~ Release time control<br>(refer to APEQ release time table in Addr 0x1A) |      |

**Addr 0x1D: APEQ Filter Control 5 for APEQ4 (BQ10)**

|      |   |         |   |   |         |   |   |   |
|------|---|---------|---|---|---------|---|---|---|
| Bit  | 7 | 6       | 5 | 4 | 3       | 2 | 1 | 0 |
| Name | X | C1C_DP4 |   |   | A1C_DP4 |   |   |   |

| Name    | Description       | Value                   | Meaning   | Ref. |
|---------|-------------------|-------------------------|---|------|
| A1C_DP4 | APEQ attack time  | <b>b'0000</b><br>b'1010 | ~ Attack time control<br>(refer to APEQ attack time table in Addr 0x1A)   |      |
| C1C_DP4 | APEQ release time | <b>b'000</b><br>b'111   | ~ Release time control<br>(refer to APEQ release time table in Addr 0x1A) |      |

**Addr 0x1E: APEQ Filter Control 6 for APEQ5 (BQ11)**

|      |   |         |   |   |         |   |   |   |
|------|---|---------|---|---|---------|---|---|---|
| Bit  | 7 | 6       | 5 | 4 | 3       | 2 | 1 | 0 |
| Name | X | C1C_DP5 |   |   | A1C_DP5 |   |   |   |

| Name    | Description       | Value                   | Meaning   | Ref. |
|---------|-------------------|-------------------------|---|------|
| A1C_DP5 | APEQ attack time  | <b>b'0000</b><br>b'1010 | ~ Attack time control<br>(refer to APEQ attack time table in Addr 0x1A)   |      |
| C1C_DP5 | APEQ release time | <b>b'000</b><br>b'111   | ~ Release time control<br>(refer to APEQ release time table in Addr 0x1A) |      |

**Addr 0x1F: APEQ Filter Control 7 for APEQ6 (BQ12)**

|      |   |         |   |   |         |   |   |   |
|------|---|---------|---|---|---------|---|---|---|
| Bit  | 7 | 6       | 5 | 4 | 3       | 2 | 1 | 0 |
| Name | X | C1C_DP6 |   |   | A1C_DP6 |   |   |   |

| Name    | Description       | Value                   | Meaning   | Ref. |
|---------|-------------------|-------------------------|---|------|
| A1C_DP6 | APEQ attack time  | <b>b'0000</b><br>b'1010 | ~ Attack time control<br>(refer to APEQ attack time table in Addr 0x1A)   |      |
| C1C_DP6 | APEQ release time | <b>b'000</b><br>b'111   | ~ Release time control<br>(refer to APEQ release time table in Addr 0x1A) |      |

**Addr 0x20: DRC Control 0**

|      |       |       |   |   |   |   |   |   |
|------|-------|-------|---|---|---|---|---|---|
| Bit  | 7     | 6     | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | CPR_L | CTS_L |   |   |   |   |   |   |

| Name  | Description                | Value                           | Meaning  | Ref. |
|-------|----------------------------|---------------------------------|--|------|
| CTS_L | DRC threshold for Low band | <b>b'0000000</b> ~<br>b'1111111 | -57 ~ 12dB unsigned 7-bit DRC threshold for 1 band mode. In 2 band mode, It will control the threshold of low band. Refer to DRC threshold table for threshold values. |      |
| CPR_L | DRC enable for Low band    | <b>b'0</b>                      | Dynamic Range Compression off  |      |
|       |                            | <b>b'1</b>                      | Dynamic Range Compression on   |      |

**Addr 0x21: DRC Control 1**

|      |   |       |   |   |       |   |   |   |
|------|---|-------|---|---|-------|---|---|---|
| Bit  | 7 | 6     | 5 | 4 | 3     | 2 | 1 | 0 |
| Name | X | C1C_L |   |   | A1C_L |   |   |   |

| Name  | Description                 | Value           | Meaning  | Ref. |
|-------|-----------------------------|-----------------|--|------|
| A1C_L | DRC attack time (Low band)  | b'0000 ~ b'1010 | Attack time control for 1 band mode. In 2 band mode, it will control the attack time of low band. (refer to DRC attack time table below) default = <b>b'0001</b> |      |
| C1C_L | DRC release time (Low band) | b'000 ~ b'111   | Release time control for 1 band mode. In 2 band mode, it will control the release time of low band. (refer to DRC release time table below)                      |      |

| Value of Register | Attack time 6dB, fs = 96,000 |
|-------------------|------------------------------|
| 0011              | 30msec                       |
| 0010              | 15msec                       |
| 0001              | 8msec                        |
| 0000              | 4msec                        |
| 0111              | 2msec                        |
| 0110              | 1msec                        |
| 0101              | 0.5msec                      |
| 0100              | 0.25msec                     |
| 1000              | 5msec                        |
| 1001              | 6msec                        |
| 1010              | 7msec                        |

**Table 13. DRC Attack Time Table**

| Value of Register | Release time 6dB, fs = 96,000 |
|-------------------|-------------------------------|
| 011               | 5.0sec                        |
| 010               | 2.0sec                        |
| 001               | 1.0sec                        |
| 000               | 0.5sec                        |
| 111               | 0.2sec                        |
| 110               | 0.1sec                        |
| 101               | 0.05sec                       |
| 100               | 0.025sec                      |

**Table 14. DRC Release Time Table**

**Addr 0x22: DRC Control 2**

|      |       |       |   |   |   |   |   |   |
|------|-------|-------|---|---|---|---|---|---|
| Bit  | 7     | 6     | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | CPR_H | CTS_H |   |   |   |   |   |   |

| Name  | Description                 | Value                 | Meaning  | Ref. |
|-------|-----------------------------|-----------------------|--|------|
| CTS_H | DRC threshold for High band | b'0000000 ~ b'1111111 | -57 ~ 12dB unsigned 7-bit DRC threshold for high band. It has effect only in 2 band mode. Refer to DRC threshold value table for threshold values. |      |
| CPR_H | DRC enable for High band    | b'0                   | Dynamic Range Compression off  |      |
|       |                             | b'1                   | Dynamic Range Compression on   |      |

**Addr 0x23: DRC Control 3**

|      |   |       |   |   |       |   |   |   |
|------|---|-------|---|---|-------|---|---|---|
| Bit  | 7 | 6     | 5 | 4 | 3     | 2 | 1 | 0 |
| Name | X | C1C_H |   |   | A1C_H |   |   |   |

| Name  | Description                  | Value           | Meaning   | Ref. |
|-------|------------------------------|-----------------|---|------|
| A1C_H | DRC attack time (High band)  | b'0000 ~ b'1010 | Attack time control for high band mode. It has effect only in 2 band mode. (See DRC attack time table in Addr 0x21) default = <b>b'0001</b> |      |
| C1C_H | DRC release time (High band) | b'000 ~ b'111   | Release time control for high band mode. It has effect only in 2 band mode. (refer to DRC release time table in Addr 0x21)                  |      |

**Reserved Address 0x24 ~ 0x25**

**Addr 0x26: DRC Control 6**

|      |       |       |   |   |   |   |   |   |
|------|-------|-------|---|---|---|---|---|---|
| Bit  | 7     | 6     | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | CPR_P | CTS_P |   |   |   |   |   |   |

| Name  | Description                 | Value                 | Meaning   | Ref. |
|-------|-----------------------------|-----------------------|---|------|
| CTS_P | DRC threshold for Post band | b'0000000 ~ b'1111111 | -57 ~ 12dB unsigned 7-bit DRC threshold Refer to DRC threshold table. |      |
| CPR_P | DRC enable for Post band    | b'0                   | Dynamic Range Compression off   |      |
|       |                             | b'1                   | Dynamic Range Compression on  |      |

**Addr 0x27: DRC Control 7**

|      |   |       |   |   |       |   |   |   |
|------|---|-------|---|---|-------|---|---|---|
| Bit  | 7 | 6     | 5 | 4 | 3     | 2 | 1 | 0 |
| Name | X | C1C_P |   |   | A1C_P |   |   |   |

| Name  | Description                  | Value           | Meaning  | Ref. |
|-------|------------------------------|-----------------|--|------|
| A1C_P | DRC attack time (Post band)  | b'0000 ~ b'1010 | Attack time control (refer to DRC attack time table in Addr 0x21) default = <b>b'0001</b>  |      |
| C1C_P | DRC release time (Post band) | b'000 ~ b'111   | Release time control (refer to DRC release time table in Addr 0x21) default = <b>b'100</b> |      |

**Addr 0x28: DRC Control 8**

|      |   |   |   |     |   |   |   |   |
|------|---|---|---|-----|---|---|---|---|
| Bit  | 7 | 6 | 5 | 4   | 3 | 2 | 1 | 0 |
| Name | X | X | X | DLL |   |   |   |   |

| Name | Description       | Value           | Meaning                          | Ref. |
|------|-------------------|-----------------|----------------------------------|------|
| DLL  | Delay line length | b'00000~b'10100 | Delay line length. 0~20(decimal) |      |

**Addr 0x29: DRC Control 9**

|      |     |      |      |     |   |   |   |     |
|------|-----|------|------|-----|---|---|---|-----|
| Bit  | 7   | 6    | 5    | 4   | 3 | 2 | 1 | 0   |
| Name | CCO | DTS1 | DTS2 | 2BM | X | X | X | CAS |

| Name | Description                       | Value | Meaning                            | Ref. |
|------|-----------------------------------|-------|------------------------------------|------|
| CAS  | Coupled All pass Structure enable | b'0   | Enable coupled all pass structure  |      |
|      |                                   | b'1   | Disable coupled all pass structure |      |
| 2BM  | 2band mode enable                 | b'0   | 1 band DRC                         |      |
|      |                                   | b'1   | 2 band DRC                         |      |
| DTS2 | P-DRC type select                 | b'0   | P-DRC new mode                     |      |
|      |                                   | b'1   | P-DRC old mode                     |      |
| DTS1 | LH-DRC type select                | b'0   | LH-DRC new mode                    |      |
|      |                                   | b'1   | LH-DRC old mode                    |      |
| CCO  | Clip control option               | b'0   | Clip off                           |      |
|      |                                   | b'1   | Clip on                            |      |

**Addr 0x2A: DRC Control 10**

|      |       |       |   |   |   |   |   |   |
|------|-------|-------|---|---|---|---|---|---|
| Bit  | 7     | 6     | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | CPR_S | CTS_S |   |   |   |   |   |   |

| Name  | Description                | Value                 | Meaning   | Ref. |
|-------|----------------------------|-----------------------|---|------|
| CTS_S | DRC threshold for Sub band | b'0000000 ~ b'1111111 | -57 ~ 12dB unsigned 7-bit DRC threshold for Sub band.<br>It has effect only in 3 band mode.<br>Refer to DRC threshold table for threshold values. default= <b>b'1101010</b> |      |
| CPR_S | DRC enable for Sub band    | b'0                   | Dynamic Range Compression off   |      |
|       |                            | b'1                   | Dynamic Range Compression on  |      |

**Addr 0x2B: DRC Control 11**

|      |   |       |   |   |       |   |   |   |
|------|---|-------|---|---|-------|---|---|---|
| Bit  | 7 | 6     | 5 | 4 | 3     | 2 | 1 | 0 |
| Name | X | C1C_S |   |   | A1C_S |   |   |   |

| Name  | Description                 | Value           | Meaning   | Ref. |
|-------|-----------------------------|-----------------|---|------|
| A1C_S | DRC attack time (Sub band)  | b'0000 ~ b'1010 | Attack time control for sub band mode.<br>It has effect only in 3 band mode.<br>(Refer to DRC attack time table in Addr 0x21.)<br>default = <b>b'0001</b> |      |
| C1C_S | DRC release time (Sub band) | b'000 ~ b'111   | Release time control for sub band mode.<br>It has effect only in 3 band mode.<br>(refer to DRC release time table in Addr 0x21.)                          |      |

**Addr 0x2C: DRC Control 12**

|      |   |   |   |   |   |   |      |     |
|------|---|---|---|---|---|---|------|-----|
| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0   |
| Name | X | X | X | X | X | X | DTS3 | SBM |

| Name | Description          | Value | Meaning               | Ref. |
|------|----------------------|-------|-----------------------|------|
| SBM  | Sub band mode enable | b'0   | Sub band mode Disable |      |
|      |                      | b'1   | Sub band mode Enable  |      |
| DTS3 | Sub DRC type select  | b'0   | Sub DRC new mode      |      |
|      |                      | b'1   | Sub DRC old mode      |      |

**Reserved Address 0x2D**

**Addr 0x2E : Power Meter Control**

|      |   |   |   |       |   |   |      |   |
|------|---|---|---|-------|---|---|------|---|
| Bit  | 7 | 6 | 5 | 4     | 3 | 2 | 1    | 0 |
| Name | X | X | X | PDPOS | X | X | PDCH |   |

| Name  | Description                 | Value | Meaning                            | Ref. |
|-------|-----------------------------|-------|------------------------------------|------|
| PDCH  | Power meter Detect Channel  | b'00  | L+R (default)                      |      |
|       |                             | b'01  | L channel                          |      |
|       |                             | b'10  | R channel                          |      |
| PDPOS | Power meter Detect Position | b'0   | After volume (default)             |      |
|       |                             | b'1   | Before volume (from digital input) |      |

**Addr 0x2F : Power Meter (read only)**

|      |             |   |   |   |   |   |   |   |
|------|-------------|---|---|---|---|---|---|---|
| Bit  | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | Power meter |   |   |   |   |   |   |   |



**Addr 0x30: Soft Volume Control**

| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1   | 0 |
|------|---|---|---|---|---|---|-----|---|
| Name | X | X | X | X | X | X | SVI |   |

| Name | Description        | Value       | Meaning                    | Ref. |
|------|--------------------|-------------|----------------------------|------|
| SVI  | Soft volume change | <b>b'00</b> | Medium speed               |      |
|      |                    | b'01        | High speed                 |      |
|      |                    | b'10        | Low speed                  |      |
|      |                    | b'11        | soft volume change disable |      |

**Reserved Address 0x31 ~ 0x32**

**Addr 0x33 : Soft Mute Control**

| Bit  | 7   | 6 | 5 | 4 | 3 | 2 | 1   | 0   |
|------|-----|---|---|---|---|---|-----|-----|
| Name | SMH | X | X | X | X | X | SM2 | SM1 |

| Name | Description            | Value      | Meaning                    | Ref. |
|------|------------------------|------------|----------------------------|------|
| SMn  | Softmute               | b'0        | increase for channel n     |      |
|      |                        | b'1        | decrease for channel n     |      |
| SMH  | Soft Mute Change speed | <b>b'0</b> | 42/46 msec (at 96/88.2kHz) |      |
|      |                        | b'1        | Hard change                |      |

**Addr 0x34 : PWM Switching On/Off Control**

| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
|------|---|---|---|---|---|---|------|------|
| Name | X | X | X | X | X | X | POF2 | POF1 |

| Name | Description                     | Value      | Meaning                     | Ref. |
|------|---------------------------------|------------|-----------------------------|------|
| POFn | Switching output On/off control | b'0        | Channel n PWM switching on  |      |
|      |                                 | <b>b'1</b> | Channel n PWM switching off |      |

**Addr 0x35 : PWM\_MASK Control 0**

| Bit  | 7 | 6 | 5 | 4 | 3   | 2     | 1    | 0 |
|------|---|---|---|---|-----|-------|------|---|
| Name | X | X | X | X | SRD | FPMLD | PWMM |   |

| Name  | Description                         | Value       | Meaning                                      | Ref. |
|-------|-------------------------------------|-------------|--|------|
| PWMM  | PWM MASK register                   | <b>b'10</b> | PWM MASK output is low.                      |      |
|       |                                     | Otherwise   | PWM MASK output is high.                     |      |
| FPMLD | Permanent PWM_MASK Low disable flag | <b>b'0</b>  | No effect                                    |      |
|       |                                     | b'1         | Reset the Auto PWM_MASK restore counter to 0 |      |
| SRD   | FAULT disable                       | <b>b'0</b>  | FAULT is effective for PROTECT               |      |
|       |                                     | b'1         | FAULT is ineffective for PROTECT             |      |

**Addr 0x36 : PWM\_MASK Control 1**

| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1   | 0   |
|------|---|---|---|---|---|---|-----|-----|
| Name | X | X | X | X | X | X | APM | POF |

| Name | Description   | Value      | Meaning   | Ref. |
|------|---------------|------------|---|------|
| POF  | PWM off flag  | <b>b'0</b> | Even if Auto PWM_MASK condition is met, the PWM output of all channels is not affected.   |      |
|      |               | b'1        | When Auto PWM_MASK condition is met, the PWM output of all channels goes to the defined state which is set by the PWM off state control registers (Addr 0x37 & 0x6F). |      |
| APM  | PWM_MASK flag | <b>b'0</b> | Even if Auto PWM_MASK condition is met, the PWM_MASK output of all channels is not affected.  |      |
|      |               | b'1        | When Auto PWM_MASK condition is met, the PWM_MASK output goes to Low state.   |      |

**Addr 0x37 : PWM\_MASK Control 2**

|      |   |       |       |       |   |       |       |       |
|------|---|-------|-------|-------|---|-------|-------|-------|
| Bit  | 7 | 6     | 5     | 4     | 3 | 2     | 1     | 0     |
| Name | X | VMSK2 | VMSK1 | VMSK0 | X | PMSK2 | PMSK1 | PMSK0 |

| Name  | Description                    | Value | Meaning   | Ref. |
|-------|--------------------------------|-------|---|------|
| PMSKn | Masking bit of PWM off control | b'0   | Mask bit indicating the validity of n-th bit of Addr 0x75 system register: If the n-th bit of this register is zero, the n-th bit of Addr 0x75 system register is invalid. The n-th bit of Addr 0x75 is valid only when the n-th mask bit is one. |      |
|       |                                | b'1   |   |      |
| VMSKn | Masking bit of PWM_MASK signal | b'0   |   |      |
|       |                                | b'1   |   |      |

**Addr 0x38 : PWM\_MASK Control 3**

|      |     |   |       |   |   |     |   |   |
|------|-----|---|-------|---|---|-----|---|---|
| Bit  | 7   | 6 | 5     | 4 | 3 | 2   | 1 | 0 |
| Name | IRC |   | AVRCT |   |   | PHT |   |   |

| Name  | Description                                  | Value        | Meaning                    | Ref. |
|-------|--|--------------|----------------------------|------|
| PHT   | PWM_MASK Low Hold Time                       | b'000        | 0.5 msec Hold Time         |      |
|       |  | b'001        | 1 msec Hold Time           |      |
|       |  | b'010        | 2 msec Hold Time           |      |
|       |  | <b>b'011</b> | 4 msec Hold Time (Default) |      |
|       |  | b'100        | 8 msec Hold Time           |      |
|       |  | b'101        | 16msec Hold Time           |      |
| AVRCT | Auto PWM_MASK Restore Counter Threshold      | b'000        | 2                          |      |
|       |  | <b>b'001</b> | 5 (Default)                |      |
|       |  | b'010        | 10                         |      |
|       |  | b'011        | 15                         |      |
|       |  | b'100        | 20                         |      |
|       |  | b'101        | 25                         |      |
| IRC   | Auto PWM_MASK Restore Interval Ratio Control | <b>b'00</b>  | 2 (Default)                |      |
|       |  | b'01         | 4                          |      |
|       |  | b'111        | Infinity                   |      |

**Addr 0x39 : PWM\_MASK Control 4**

|      |     |     |   |   |   |     |   |   |
|------|-----|-----|---|---|---|-----|---|---|
| Bit  | 7   | 6   | 5 | 4 | 3 | 2   | 1 | 0 |
| Name | SHE | POE | X | X | X | HT2 |   |   |

| Name | Description  | Value        | Meaning                      | Ref. |
|------|--|--------------|------------------------------|------|
| HT2  | Hold Time 2 apply start point (restore counter)              | b'000        | 100 msec Hold Time           |      |
|      |  | b'001        | 200 msec Hold Time           |      |
|      |  | b'010        | 400 msec Hold Time           |      |
|      |  | <b>b'011</b> | 600 msec Hold Time (Default) |      |
|      |  | b'100        | 800 msec Hold Time           |      |
|      |  | b'101        | 1 sec Hold Time              |      |
|      |  | b'110        | 2 sec Hold Time              |      |
|      |  | b'111        | 4 sec Hold Time              |      |
| POE  | PWM off when Fault detected and PWM on when PWM_MASK recover | b'0          | Disable                      |      |
|      |  | <b>b'1</b>   | Enable (Default)             |      |
| SHE  | Second Hold time Enable                                      | <b>b'0</b>   | Disable                      |      |
|      |  | b'1          | Enable                       |      |

**Addr 0x3A: Auto-Mute Control for CH1 & CH2**

|      |   |      |    |    |   |   |   |   |
|------|---|------|----|----|---|---|---|---|
| Bit  | 7 | 6    | 5  | 4  | 3 | 2 | 1 | 0 |
| Name | X | EAMC | II | AT |   |   |   |   |

| Name | Description                   | Value                  | Meaning  | Ref. |
|------|-------------------------------|------------------------|--|------|
| AT   | Auto-mute detection threshold | <b>b'0000</b> ~ b'1111 | Unsigned integer between 0 and 15 Refer to Auto Mute detection threshold table for threshold values. |      |
| II   | Auto-mute response time       | <b>b'00</b>            | 5 msec   |      |
|      |                               | b'01                   | 50 msec  |      |
|      |                               | b'10                   | 500 msec   |      |
|      |                               | b'11                   | 2 sec  |      |
| EAMC | Effect of Auto-mute condition | <b>b'0</b>             | Auto mute disable (No-Effect)  |      |
|      |                               | b'1                    | Stop PWM switching when auto-mute condition is met.  |      |

**Reserved Address 0x3B**

**Addr 0x3C: CH1&CH2 Prescaler Value Control**

|      |      |   |   |   |   |   |   |   |
|------|------|---|---|---|---|---|---|---|
| Bit  | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PS12 |   |   |   |   |   |   |   |

| Name | Description     | Value                   | Meaning               | Ref. |
|------|-----------------|-------------------------|-----------------------|------|
| PS12 | Prescaler value | b'00000000 ~ b'11111111 | default = <b>0x4C</b> |      |

**Reserved Address 0x3D**

**Addr 0x3E: PWM Output Port Control for PWM Port 1A & 1B**

|      |   |   |       |   |   |       |   |   |
|------|---|---|-------|---|---|-------|---|---|
| Bit  | 7 | 6 | 5     | 4 | 3 | 2     | 1 | 0 |
| Name | X | X | OPM1B |   |   | OPM1A |   |   |

| Name  | Description                                  | Value        | Meaning                           | Ref. |
|-------|--|--------------|-----------------------------------|------|
| OPM1A | Select source channel for PWM output port 1A | <b>b'000</b> | PWM1A is connected to PWM port 1A |      |
|       |  | b'001        | PWM1B is connected to PWM port 1A |      |
|       |  | b'010        | PWM2A is connected to PWM port 1A |      |
|       |  | b'011        | PWM2B is connected to PWM port 1A |      |
| OPM1B | Select source channel for PWM output port 1B | b'000        | PWM1A is connected to PWM port 1B |      |
|       |  | <b>b'001</b> | PWM1B is connected to PWM port 1B |      |
|       |  | b'010        | PWM2A is connected to PWM port 1B |      |
|       |  | b'011        | PWM2B is connected to PWM port 1B |      |

**Addr 0x3F: PWM Output Port Control for PWM Port 2A & 2B**

|      |   |   |       |   |   |       |   |   |
|------|---|---|-------|---|---|-------|---|---|
| Bit  | 7 | 6 | 5     | 4 | 3 | 2     | 1 | 0 |
| Name | X | X | OPM2B |   |   | OPM2A |   |   |

| Name  | Description                                  | Value        | Meaning                           | Ref. |
|-------|--|--------------|-----------------------------------|------|
| OPM2A | Select source channel for PWM output port 2A | b'000        | PWM1A is connected to PWM port 2A |      |
|       |  | b'001        | PWM1B is connected to PWM port 2A |      |
|       |  | <b>b'010</b> | PWM2A is connected to PWM port 2A |      |
|       |  | b'011        | PWM2B is connected to PWM port 2A |      |
| OPM2B | Select source channel for PWM output port 2B | b'000        | PWM1A is connected to PWM port 2B |      |
|       |  | b'001        | PWM1B is connected to PWM port 2B |      |
|       |  | b'010        | PWM2A is connected to PWM port 2B |      |
|       |  | <b>b'011</b> | PWM2B is connected to PWM port 2B |      |

**Addr 0x40: NS Soft Mute Control**

| Bit      | 7                                      | 6             | 5   | 4      | 3       | 2 | 1 | 0 |
|----------|--|---------------|---|--------|---------|---|---|---|
| Name     | X                                      | X             | Time_Lim  | Enable | CNT_THR |   |   |   |
| Name     | Description                            | Value         | Meaning   |        | Ref.    |   |   |   |
| CNT_THR  | Minimum counting value                 | b'0000~b'1111 | Minimum counting value of continuous zeros for forcing NS_OUT as 0. default = <b>b'0110</b> |        |         |   |   |   |
| Enable   | Enable NS soft mute                    | b'0           | Disable   |        |         |   |   |   |
|          |  | b'1           | Enable  |        |         |   |   |   |
| Time_Lim | Time limit on finding continuous zeros | b'0           | Time Limit = 200ms  |        |         |   |   |   |
|          |  | b'1           | Time Limit = 400ms  |        |         |   |   |   |

**Addr 0x41: Modulation Index & NS-Type Control**

| Bit       | 7  | 6     | 5  | 4  | 3    | 2         | 1    | 0 |
|-----------|--|-------|--|----|------|-----------|------|---|
| Name      | X  | M0    |  | FB | X    | NTF_Order | MD12 |   |
| Name      | Description  | Value | Meaning                                    |    | Ref. |           |      |   |
| MD12      | Modulation index control by Minimum pulse width for Ch 1&2 | b'00  | Minimum pulse width = 80 ns                |    |      |           |      |   |
|           |  | b'01  | Minimum pulse width = 60 ns                |    |      |           |      |   |
|           |  | b'10  | Minimum pulse width = 40 ns                |    |      |           |      |   |
|           |  | b'11  | Minimum pulse width = 20 ns                |    |      |           |      |   |
| NTF_Order | Select NTF Order   | b'0   | NTF Order = 4                              |    |      |           |      |   |
|           |  | b'1   | NTF Order = 5                              |    |      |           |      |   |
| FB        | Feed Back on/off   | b'0   | NS Feed Back off                           |    |      |           |      |   |
|           |  | b'1   | NS Feed Back on                            |    |      |           |      |   |
| M0        | Dither Position Selector                                   | b'00  | No left shift on dither value = Dither off |    |      |           |      |   |
|           |  | b'01  | 1bit left shift on dither value            |    |      |           |      |   |
|           |  | b'10  | 2bit left shift on dither value            |    |      |           |      |   |
|           |  | b'11  | 3bit left shift on dither value            |    |      |           |      |   |

**Addr 0x42: NS Feedback Limit**

| Bit   | 7               | 6                   | 5                                     | 4 | 3    | 2 | 1 | 0 |
|-------|-----------------|---------------------|---------------------------------------|---|------|---|---|---|
| Name  | X               | FBMAX               |                                       |   |      |   |   |   |
| Name  | Description     | Value               | Meaning                               |   | Ref. |   |   |   |
| FBMAX | Feedback on/off | b'0000000~b'1111111 | Feedback limit, default = <b>0x04</b> |   |      |   |   |   |

**Addr 0x43: Miscellaneous PWM Control**

| Bit  | 7                              | 6     | 5                                     | 4 | 3    | 2   | 1  | 0 |
|------|--------------------------------|-------|---------------------------------------|---|------|-----|----|---|
| Name | X                              | X     | X                                     | X | BHL  | AHL | MD |   |
| Name | Description                    | Value | Meaning                               |   | Ref. |     |    |   |
| MD   | PWM output mode                | b'00  | AD mode with asynchronous signal pair |   |      |     |    |   |
|      |                                | b'01  | AD mode with synchronous signal pair  |   |      |     |    |   |
|      |                                | b'10  | PWM D-BTL MODE (see 0x45)             |   |      |     |    |   |
| AHL  | A-out state When switching off | b'0   | Low                                   |   |      |     |    |   |
|      |                                | b'1   | High                                  |   |      |     |    |   |
| BHL  | B-out state when switching off | b'0   | Low                                   |   |      |     |    |   |
|      |                                | b'1   | High                                  |   |      |     |    |   |

**Addr 0x44: PWM D-BTL MODE Control 0**

| Bit  | 7                           | 6         | 5   | 4 | 3    | 2 | 1 | 0 |
|------|-----------------------------|-----------|---|---|------|---|---|---|
| Name | X                           | MLP       |   |   |      |   |   |   |
| Name | Description                 | Value     | Meaning   |   | Ref. |   |   |   |
| MLP  | Minimum Linear pulse length | b'0001110 | Unsigned 0~64 (In PWM768kHz, MLP is needed to be set as smaller one satisfied MLP>MPW/10ns) |   |      |   |   |   |

**Addr 0x45: PWM D-BTL MODE Control 1**

|      |   |   |   |   |   |   |     |   |
|------|---|---|---|---|---|---|-----|---|
| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1   | 0 |
| Name | X | X | X | X | X | X | NSS |   |

| Name | Description | Value       | Meaning                   | Ref. |
|------|-------------|-------------|---------------------------|------|
| NSS  | NS Select   | <b>b'00</b> | 7bits NS (AD mode)        |      |
|      |             | b'01        | Reserved                  |      |
|      |             | b'10        | 8bits NS                  |      |
|      |             | b'11        | New 8bits NS (D-BTL mode) |      |

**Reserved Address 0x46 ~ 0x49**

**Addr 0x4A: Soft Start Control 0**

|      |     |     |   |   |   |   |   |   |
|------|-----|-----|---|---|---|---|---|---|
| Bit  | 7   | 6   | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PSE | SRT |   |   |   |   |   |   |

| Name | Description           | Value                 | Meaning   | Ref. |
|------|-----------------------|-----------------------|---|------|
| SRT  | Step Repeat Time      | b'000000<br>~b'111111 | Repeat time of each step (default = <b>b'0010000</b> – means repeat 17 times) |      |
| PSE  | PWM soft start Enable | b'0                   | Disable   |      |
|      |                       | <b>b'1</b>            | Enable (only under AD mode)   |      |

**Addr 0x4B: Soft Start Control 1**

|      |   |   |   |   |   |   |       |   |
|------|---|---|---|---|---|---|-------|---|
| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0 |
| Name | X | X | X | X | X | X | MP_PD |   |

| Name  | Description                              | Value       | Meaning                   | Ref. |
|-------|--|-------------|---------------------------|------|
| MP_PD | Soft start minimum pulse of Power device | b'00        | First pulse width = 20 ns |      |
|       |  | <b>b'01</b> | First pulse width = 40 ns |      |
|       |  | b'10        | First pulse width = 60 ns |      |
|       |  | b'11        | First pulse width = 80 ns |      |

**Reserved Address 0x4C ~ 0x4F**

**Addr 0x50: AD DC Protection Control 0**

|      |     |   |   |   |     |   |   |   |
|------|-----|---|---|---|-----|---|---|---|
| Bit  | 7   | 6 | 5 | 4 | 3   | 2 | 1 | 0 |
| Name | PDH |   |   |   | PDL |   |   |   |

| Name | Description   | Value         | Meaning | Ref. |
|------|---------------|---------------|---------|------|
| PDL  | PWM Duty Low  | b'0000        | 40%     |      |
|      |               | b'0001        | 35%     |      |
|      |               | <b>b'0010</b> | 30%     |      |
|      |               | b'0011        | 25%     |      |
|      |               | b'0100        | 20%     |      |
|      |               | b'0101        | 15%     |      |
|      |               | b'0110        | 10%     |      |
|      |               | b'0111        | 5%      |      |
|      |               | b'1000        | 45%     |      |
| PDH  | PWM Duty High | b'0000        | 60%     |      |
|      |               | b'0001        | 65%     |      |
|      |               | <b>b'0010</b> | 70%     |      |
|      |               | b'0011        | 75%     |      |
|      |               | b'0100        | 80%     |      |
|      |               | b'0101        | 85%     |      |
|      |               | b'0110        | 90%     |      |
|      |               | b'0111        | 95%     |      |
|      |               | b'1000        | 55%     |      |

**Addr 0x51: D-BTL DC Protection Control 1**

|      |   |   |   |   |      |   |   |   |
|------|---|---|---|---|------|---|---|---|
| Bit  | 7 | 6 | 5 | 4 | 3    | 2 | 1 | 0 |
| Name | X | X | X | X | MLPA |   |   |   |

| Name   | Description    | Value         | Meaning | Ref. |
|--------|----------------|---------------|---------|------|
| MLPA   | D-BTL Duty MLP | <b>b'0000</b> | 5%      |      |
|        |                | b'0001        | 10%     |      |
|        |                | b'0010        | 15%     |      |
|        |                | b'0011        | 20%     |      |
|        |                | b'0100        | 25%     |      |
|        |                | b'0101        | 30%     |      |
|        |                | b'0110        | 35%     |      |
|        |                | b'0111        | 40%     |      |
|        |                | b'1000        | 45%     |      |
| b'1001 | 50%            |               |         |      |

**Addr 0x52: DC Protection Control 2**

|      |     |     |   |   |   |     |     |     |
|------|-----|-----|---|---|---|-----|-----|-----|
| Bit  | 7   | 6   | 5 | 4 | 3 | 2   | 1   | 0   |
| Name | SRE | SRF | X | X | X | PFE | DFE | MFE |

| Name | Description                  | Value      | Meaning                           | Ref. |
|------|------------------------------|------------|-----------------------------------|------|
| MFE  | PWM duty Error Enable        | <b>b'0</b> | PWM duty Error Disable            |      |
|      |                              | b'1        | PWM duty Error Enable             |      |
| DFE  | DRC Coefficient Error Enable | <b>b'0</b> | MDRC Coefficient Error Disable    |      |
|      |                              | b'1        | MDRC Coefficient Error Enable     |      |
| PFE  | PBQ Coefficient Error Enable | <b>b'0</b> | PBQ Coefficient Error Disable     |      |
|      |                              | b'1        | PBQ Coefficient Error Enable      |      |
| SRF  | DC Soft Reset Flag           | <b>b'0</b> |                                   |      |
|      |                              | b'1        | DC Soft Reset start in Modulation |      |
| SRE  | DC Soft Reset Enable         | <b>b'0</b> | DC Soft Reset Flag Disable        |      |
|      |                              | b'1        | DC Soft Reset Flag Enable         |      |

**Addr 0x53: DC Protection Control 3**

|      |   |   |      |   |   |   |   |   |
|------|---|---|------|---|---|---|---|---|
| Bit  | 7 | 6 | 5    | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | PCS3 |   |   |   |   |   |

| Name | Description             | Value | Meaning               | Ref. |
|------|-------------------------|-------|-----------------------|------|
| PCS3 | PBQ RX Check Sum(29:24) |       | default = <b>0x32</b> |      |

**Addr 0x54: DC Protection Control 4**

|      |      |   |   |   |   |   |   |   |
|------|------|---|---|---|---|---|---|---|
| Bit  | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PCS2 |   |   |   |   |   |   |   |

| Name | Description              | Value | Meaning               | Ref. |
|------|--------------------------|-------|-----------------------|------|
| PCS2 | PBQ RX Check Sum (23:16) |       | default = <b>0x00</b> |      |

**Addr 0x55: DC Protection Control 5**

|      |      |   |   |   |   |   |   |   |
|------|------|---|---|---|---|---|---|---|
| Bit  | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PCS1 |   |   |   |   |   |   |   |

| Name | Description             | Value | Meaning               | Ref. |
|------|-------------------------|-------|-----------------------|------|
| PCS1 | PBQ RX Check Sum (15:8) |       | default = <b>0x00</b> |      |

**Addr 0x56: DC Protection Control 6**

|      |      |   |   |   |   |   |   |   |
|------|------|---|---|---|---|---|---|---|
| Bit  | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PCS0 |   |   |   |   |   |   |   |

| Name | Description            | Value | Meaning               | Ref. |
|------|------------------------|-------|-----------------------|------|
| PCS0 | PBQ RX Check Sum (7:0) |       | default = <b>0x00</b> |      |

**Addr 0x57: DC Protection Control 7**

|      |   |   |      |   |   |   |   |   |
|------|---|---|------|---|---|---|---|---|
| Bit  | 7 | 6 | 5    | 4 | 3 | 2 | 1 | 0 |
| Name | X | X | DCS3 |   |   |   |   |   |

| Name | Description               | Value | Meaning               | Ref. |
|------|---------------------------|-------|-----------------------|------|
| DCS3 | MDRC RX Check Sum (29:24) |       | default = <b>0x14</b> |      |

**Addr 0x58: DC Protection Control 8**

|      |      |   |   |   |   |   |   |   |
|------|------|---|---|---|---|---|---|---|
| Bit  | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | DCS2 |   |   |   |   |   |   |   |

| Name | Description               | Value | Meaning               | Ref. |
|------|---------------------------|-------|-----------------------|------|
| DCS2 | MDRC RX Check Sum (23:16) |       | default = <b>0x8E</b> |      |

**Addr 0x59: DC Protection Control 9**

|      |      |   |   |   |   |   |   |   |
|------|------|---|---|---|---|---|---|---|
| Bit  | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | DCS1 |   |   |   |   |   |   |   |

| Name | Description              | Value | Meaning               | Ref. |
|------|--------------------------|-------|-----------------------|------|
| DCS1 | MDRC RX Check Sum (15:8) |       | default = <b>0x9C</b> |      |

**Addr 0x5A: DC Protection Control 10**

|      |      |   |   |   |   |   |   |   |
|------|------|---|---|---|---|---|---|---|
| Bit  | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | DCS0 |   |   |   |   |   |   |   |

| Name | Description             | Value | Meaning               | Ref. |
|------|-------------------------|-------|-----------------------|------|
| DCS0 | MDRC RX Check Sum (7:0) |       | default = <b>0x10</b> |      |

**Addr 0x5B: DC Protection Control 11 (read only)**

|      |   |   |   |   |   |     |     |     |
|------|---|---|---|---|---|-----|-----|-----|
| Bit  | 7 | 6 | 5 | 4 | 3 | 2   | 1   | 0   |
| Name | X | X | X | X | X | PEF | DEF | MEF |

| Name | Description                | Value      | Meaning                | Ref. |
|------|----------------------------|------------|------------------------|------|
| MEF  | PWM duty Error Flag        | <b>b'0</b> |                        |      |
|      |                            | b'1        | PWM duty Error         |      |
| DEF  | DRC Coefficient Error Flag | <b>b'0</b> |                        |      |
|      |                            | b'1        | MDRC Coefficient Error |      |
| PEF  | PEQ Coefficient Error Flag | <b>b'0</b> |                        |      |
|      |                            | b'1        | PEQ Coefficient Error  |      |

**Addr 0x5C: Checksum Download Type Control**

|      |   |   |   |   |   |   |   |     |
|------|---|---|---|---|---|---|---|-----|
| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0   |
| Name | X | X | X | X | X | X | X | CDT |

| Name | Description            | Value | Meaning                               | Ref. |
|------|------------------------|-------|---------------------------------------|------|
| CDT  | Checksum download type | b'0   | 1byte * 4 (addr 0x53~0x56, 0x57~0x5A) |      |
|      |                        | b'1   | 4byte (Coefficient mode)              |      |

**Addr 0x5D: Driver Control**

|      |   |   |   |   |   |   |     |      |
|------|---|---|---|---|---|---|-----|------|
| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1   | 0    |
| Name | X | X | X | X | X | X | KMS | SHDN |

| Name | Description            | Value | Meaning                        | Ref. |
|------|------------------------|-------|--------------------------------|------|
| SHDN | Shutdown               | b'0   | SHDN pin go to low             |      |
|      |                        | b'1   | SHDN pin go to high            |      |
| KMS  | PWM MASK output select | b'0   | PWM_MASK0,1 pin <= PWM_MASK0,1 |      |
|      |                        | b'1   | PWM_MASK0,1 pin <= SHDN        |      |

**Reserved Address 0x5E ~ 0x5F**

**Addr 0x60: SSRC Control 0**

|      |   |   |       |   |       |       |   |   |
|------|---|---|-------|---|-------|-------|---|---|
| Bit  | 7 | 6 | 5     | 4 | 3     | 2     | 1 | 0 |
| Name | X | X | DCESW | X | FSFHM | FSFSM | X | X |

| Name  | Description                               | Value | Meaning                                | Ref. |
|-------|---|-------|--|------|
| FSFSM | frequency stable effect on soft mute flag | b'0   | no effect on soft mute flag            |      |
|       |   | b'1   | soft mute flag = 1 when unstable state |      |
| FSFHM | frequency stable effect on hard mute flag | b'0   | no effect on hard mute flag            |      |
|       |   | b'1   | hard mute flag = 1 when unstable state |      |
| DCESW | DC Check Enable of SRC WCK                | b'0   | DC Check Disable in SRC WCK            |      |
|       |   | b'1   | DC Check Enable in SRC WCK             |      |

**Addr 0x61: SSRC Control 1**

|      |   |   |   |   |     |   |   |   |
|------|---|---|---|---|-----|---|---|---|
| Bit  | 7 | 6 | 5 | 4 | 3   | 2 | 1 | 0 |
| Name | X | X | X | X | FVT |   |   |   |

| Name | Description                   | Value           | Meaning  | Ref. |
|------|-------------------------------|-----------------|--|------|
| FVT  | Frequency variation threshold | b'0000 ~ b'1111 | threshold value for frequency stable check (unsigned integer) default : b'0111 |      |

**Reserved Address 0x62 ~ 0x65**

**Addr 0x66: I<sup>2</sup>C Glitch Filter**

|      |     |     |   |   |   |   |   |   |
|------|-----|-----|---|---|---|---|---|---|
| Bit  | 7   | 6   | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | GFO | DUR |   |   |   |   |   |   |

| Name | Description                  | Value                 | Meaning  | Ref. |
|------|------------------------------|-----------------------|--|------|
| DUR  | glitch width                 | b'0000000 ~ b'1111111 | minimum pulse width = DUR + 20 ns<br>reset default = 15 * 10 ns<br>(DUR default = b'0001111) |      |
|      |                              | b'0                   | Glitch filter on   |      |
| GFO  | Glitch filter enable/disable | b'0                   | Glitch filter on   |      |
|      |                              | b'1                   | Bypass   |      |

**Reserved Address 0x67**



**Addr 0x68: PWM Phase Control**

|      |     |   |   |   |     |   |   |   |
|------|-----|---|---|---|-----|---|---|---|
| Bit  | 7   | 6 | 5 | 4 | 3   | 2 | 1 | 0 |
| Name | PPC |   |   |   | PFC |   |   |   |

| Name | Description            | Value           | Meaning   | Ref.  |
|------|------------------------|-----------------|---|---|
| PFC  | PWM phase Fine Control | b'0000 ~ b'1001 | Range is 0°~14.94° with 1.66° step (In PWM768kHz, PFC range is 0~4 with 3.78° step) | In Single ended mode, fixed as PFC = b'0000, and PPC = b'0110 (90°) |
| PPC  | PWM Phase Control      | b'0000 ~ b'1100 | Range is 0°~180° with 15° step. default = b'0110 (90°)                              |   |

**Reserved Address 0x69 ~ 0x6D**

**Addr 0x6E Watch Dog Error System Status (read only)**

|      |   |   |   |   |   |     |     |     |
|------|---|---|---|---|---|-----|-----|-----|
| Bit  | 7 | 6 | 5 | 4 | 3 | 2   | 1   | 0   |
| Name | X | X | X | X | X | IWK | IBK | WDE |

| Name | Description           | Value | Meaning             | Ref. |
|------|-----------------------|-------|---------------------|------|
| WDE  | Watch Dog Ratio Error | b'0   |                     |      |
|      |                       | b'1   | Watch Dog Error     |      |
| IBK  | IIS BCK Ratio Error   | b'0   |                     |      |
|      |                       | b'1   | IIS BCK Ratio Error |      |
| IWK  | IIS WCK Ratio Error   | b'0   |                     |      |
|      |                       | b'1   | IIS WCK Ratio Error |      |

**Addr 0x6F: PWM\_MASK Control 5**

|      |   |       |       |       |   |       |       |       |
|------|---|-------|-------|-------|---|-------|-------|-------|
| Bit  | 7 | 6     | 5     | 4     | 3 | 2     | 1     | 0     |
| Name | X | VMSK2 | VMSK1 | VMSK0 | X | PMSK2 | PMSK1 | PMSK0 |

| Name  | Description                    | Value | Meaning   | Ref. |
|-------|--------------------------------|-------|---|------|
| PMSKn | Masking bit of PWM off control | b'0   | Mask bit indicating the validity of n-th bit of Addr 0x6E system register: If the n-th bit of this register is zero, the n-th bit of Addr 0x6E system register is invalid. The n-th bit of Addr 0x6E is valid only when the n-th mask bit is one. |      |
|       |                                | b'1   |   |      |
| VMSKn | Masking bit of PWM_MASK signal | b'0   |   |      |
|       |                                | b'1   |   |      |

**Addr 0x70: System Status Register (0x6E, 0x75) Holding Control 1**

|      |      |      |      |   |   |      |       |   |
|------|------|------|------|---|---|------|-------|---|
| Bit  | 7    | 6    | 5    | 4 | 3 | 2    | 1     | 0 |
| Name | HIWK | HIBK | HWDE | X | X | HMPW | HULCK | X |

| Name  | Description                           | Value | Meaning  | Ref. |
|-------|---------------------------------------|-------|--|------|
| HULCK | Enable bit of Holding the ULCK status | b'0   | Update the new value without holding the ULCK status bit of 0x75 |      |
|       |                                       | b'1   | Hold the first different value                                   |      |
| HMPW  | Enable bit of Holding the MPW status  | b'0   | Update the new value without holding the MPW status bit of 0x75  |      |
|       |                                       | b'1   | Hold the first different value                                   |      |
| HWDE  | Enable bit of Holding the WDE status  | b'0   | Update the new value without holding the WDE status bit of 0x6E  |      |
|       |                                       | b'1   | Hold the first different value                                   |      |
| HIBK  | Enable bit of Holding the IBK status  | b'0   | Update the new value without holding the IBK status bit of 0x6E  |      |
|       |                                       | b'1   | Hold the first different value                                   |      |
| HIWK  | Enable bit of Holding the IWK status  | b'0   | Update the new value without holding the IWK status bit of 0x6E  |      |
|       |                                       | b'1   | Hold the first different value                                   |      |

**Addr 0x71: POP Control 0**

|      |     |   |   |   |   |   |   |   |
|------|-----|---|---|---|---|---|---|---|
| Bit  | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RST |   |   |   |   |   |   |   |

| Name | Description  | Value                | Meaning  | Ref. |
|------|--------------|----------------------|--|------|
| RST  | Release Time | <b>unsigned 0x10</b> | WDE becomes 0 if Watch Dog detects no error during RST*10msec after WDE has been occurred. |      |

**Addr 0x72: POP Control 1**

|      |           |   |   |   |   |   |   |   |
|------|-----------|---|---|---|---|---|---|---|
| Bit  | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | ULM[15:8] |   |   |   |   |   |   |   |

| Name | Description | Value                | Meaning                                 | Ref. |
|------|-------------|----------------------|---|------|
| ULM  |             | <b>unsigned 0x00</b> | Upper limit on ratio of BCK to CLK_FR_4 |      |

**Addr 0x73: POP Control 2**

|      |          |   |   |   |   |   |   |   |
|------|----------|---|---|---|---|---|---|---|
| Bit  | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | ULM[7:0] |   |   |   |   |   |   |   |

| Name | Description | Value                | Meaning                                 | Ref. |
|------|-------------|----------------------|---|------|
| ULM  | Upper Limit | <b>unsigned 0x20</b> | Upper limit on ratio of BCK to CLK_FR_4 |      |

**Addr 0x74: POP Control 3**

|      |          |   |   |   |   |   |   |   |     |
|------|----------|---|---|---|---|---|---|---|-----|
| Bit  | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |     |
| Name | LLM[3:0] |   |   | 0 |   | 0 |   | 0 |     |
|      |          |   |   |   |   |   |   |   | WON |

| Name | Description  | Value                  | Meaning                                 | Ref. |
|------|--------------|------------------------|---|------|
| LLM  | Lower Limit  | <b>unsigned b'1001</b> | Lower limit on ratio of BCK to CLK_FR_4 |      |
| WON  | Watch-dog On | b'0                    | OFF                                     |      |
|      |              | b'1                    | ON                                      |      |

**Addr 0x75: System Error Status (read only)**

|      |     |   |     |     |   |     |      |     |
|------|-----|---|-----|-----|---|-----|------|-----|
| Bit  | 7   | 6 | 5   | 4   | 3 | 2   | 1    | 0   |
| Name | FSI |   | PSB | PDM |   | MPW | ULCK | PPM |

| Name | Description   | Value | Meaning   | Ref. |
|------|---|-------|---|------|
| PPM  | Permanent PWMMASK Indication flag                                   | b'0   |   |      |
|      |   | b'1   | Indicated that PWM_MASK is in Permanent LOW state |      |
| ULCK | Sampled PLL Unlock error  | b'0   | PLL is locked state.                              |      |
|      |   | b'1   | PLL is unlocked state.                            |      |
| MPW  | MCK/WCK Ratio error   | b'0   | Ratio is incorrect.                               |      |
|      |   | b'1   | Ratio is correct.                                 |      |
| PDM  | Power Die Monitor (Temperature, Current, Voltage, Protection Error) | b'00  | Current protection error                          |      |
|      |   | b'01  | Voltage protection error                          |      |
|      |   | b'10  | Temperature protection error                      |      |
|      |   | b'11  | Normal state                                      |      |
| PSB  | PWM switching on/off State Bit                                      | b'0   | PWM switching off state                           |      |
|      |   | b'1   | PWM switching on state                            |      |
| FSI  | Sampling Frequency Information                                      | b'00  | 48 kHz (44.1kHz)                                  |      |
|      |   | b'01  | 96 kHz  |      |
|      |   | b'10  | 32 kHz  |      |

**Addr 0x76: Monitor**

|      |          |   |   |   |          |   |   |   |
|------|----------|---|---|---|----------|---|---|---|
| Bit  | 7        | 6 | 5 | 4 | 3        | 2 | 1 | 0 |
| Name | Monitor2 |   |   |   | Monitor1 |   |   |   |

| Name      | Description                                    | Value         | Meaning                    | Ref. |
|-----------|--|---------------|----------------------------|------|
| Monitor 1 | This output doesn't come through Power Device. | b'0000        | Reserved                   |      |
|           |  | <b>b'0001</b> | Pwm1a=> Monitor 1 pin      |      |
|           |  | b'0010        | Pwm1b => Monitor 1 pin     |      |
|           |  | b'0011        | pwm2a => Monitor 1 pin     |      |
|           |  | b'0100        | Pwm2b => Monitor 1 pin     |      |
|           |  | b'1111        | SDATA out => Monitor 1 pin |      |
| Monitor 2 | This output doesn't come through Power Device. | b'0000        | Reserved                   |      |
|           |  | b'0001        | Pwm1a=> Monitor 2 pin      |      |
|           |  | b'0010        | Pwm1b => Monitor 2 pin     |      |
|           |  | <b>b'0011</b> | pwm2a => Monitor 2 pin     |      |
|           |  | b'0100        | Pwm2b => Monitor 2 pin     |      |
|           |  | b'1111        | SDATA out => Monitor 2 pin |      |

**Reserved Address 0x77 ~ 0x7B**

**Addr 0x7C: IIS Sdata\_Out Control**

|      |   |   |   |   |   |   |   |         |
|------|---|---|---|---|---|---|---|---------|
| Bit  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0       |
| Name | X | X | X | X | X | X | X | OUT_SEL |

| Name    | Description             | Value      | Meaning                                | Ref. |
|---------|-------------------------|------------|--|------|
| OUT_SEL | Select data for IIS OUT | <b>b'0</b> | Data after soft mute stage is selected |      |
|         |                         | b'1        | Data before EQ stage is selected       |      |

**Reserved Address 0x7D**

**Addr 0x7E: Bi-Quad Filter Coefficient Page**

|      |   |   |   |   |        |   |     |     |
|------|---|---|---|---|--------|---|-----|-----|
| Bit  | 7 | 6 | 5 | 4 | 3      | 2 | 1   | 0   |
| Name | X | X | X | X | APEQ_P | X | CH2 | CH1 |

| Name   | Description                                  | Value      | Meaning                                  | Ref. |
|--------|--|------------|--|------|
| CH1    | Coefficient write enable                     | <b>b'0</b> | Disable coefficient write for ch1        |      |
|        |  | b'1        | Enable coefficient write for ch1         |      |
| CH2    | Coefficient write enable                     | <b>b'0</b> | Disable coefficient write for ch2        |      |
|        |  | b'1        | Enable coefficient write for ch2         |      |
| APEQ_P | Coefficient write enable for APEQ Parameters | <b>b'0</b> | Disable coefficient write for APEQ Para. |      |
|        |  | b'1        | Enable coefficient write for APEQ Para.  |      |

Note : When writing into BQ1~BQ6 coefficients, Should write for both ch1 and ch2 separately.  
 When writing into BQ7~BQ12 coefficients, Just write for ch1.  
 (BQ7~BQ12 coefficients are same for both CH1 and CH2) When writing into APEQ Parameters, Just write for APEQ\_P.

**Coefficient Mode:**

0x00 ~ 0x31: BQ1 ~BQ10  
0x32 ~ 0x4F: QMF\_BQ1 ~ 6  
0x50 ~ 0x52: Loudness filter gain 1 ~ 3  
0x53 ~ 0x57 : Reserved  
0x58 : Power Meter Gain  
0x59 : Reserved  
0x5A : BQ Check sum  
0x5B : DRC Check sum  
0x5C ~ 0x65: BQ11 ~ BQ12  
  
0x00 ~ 0x24: APEQ Parameters

CONFIDENTIAL

**B. Configuration Register Value Reference**

**Table 15. Master Volume**

| Index | dB    | Index | dB    | Index | dB    | Index | dB    | Index | dB     | Index | dB     |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|-------|--------|
| 0xFF  | 0.0   | 0xD4  | -21.5 | 0xA9  | -43.0 | 0x7E  | -64.5 | 0x53  | -86.0  | 0x28  | -107.5 |
| 0xFE  | -0.5  | 0xD3  | -22.0 | 0xA8  | -43.5 | 0x7D  | -65.0 | 0x52  | -86.5  | 0x27  | -108.0 |
| 0xFD  | -1.0  | 0xD2  | -22.5 | 0xA7  | -44.0 | 0x7C  | -65.5 | 0x51  | -87.0  | 0x26  | -108.5 |
| 0xFC  | -1.5  | 0xD1  | -23.0 | 0xA6  | -44.5 | 0x7B  | -66.0 | 0x50  | -87.5  | 0x25  | -109.0 |
| 0xFB  | -2.0  | 0xD0  | -23.5 | 0xA5  | -45.0 | 0x7A  | -66.5 | 0x4F  | -88.0  | 0x24  | -109.5 |
| 0xFA  | -2.5  | 0xCF  | -24.0 | 0xA4  | -45.5 | 0x79  | -67.0 | 0x4E  | -88.5  | 0x23  | -110.0 |
| 0xF9  | -3.0  | 0xCE  | -24.5 | 0xA3  | -46.0 | 0x78  | -67.5 | 0x4D  | -89.0  | 0x22  | -110.5 |
| 0xF8  | -3.5  | 0xCD  | -25.0 | 0xA2  | -46.5 | 0x77  | -68.0 | 0x4C  | -89.5  | 0x21  | -111.0 |
| 0xF7  | -4.0  | 0xCC  | -25.5 | 0xA1  | -47.0 | 0x76  | -68.5 | 0x4B  | -90.0  | 0x20  | -111.5 |
| 0xF6  | -4.5  | 0xCB  | -26.0 | 0xA0  | -47.5 | 0x75  | -69.0 | 0x4A  | -90.5  | 0x1F  | -112.0 |
| 0xF5  | -5.0  | 0xCA  | -26.5 | 0x9F  | -48.0 | 0x74  | -69.5 | 0x49  | -91.0  | 0x1E  | -112.5 |
| 0xF4  | -5.5  | 0xC9  | -27.0 | 0x9E  | -48.5 | 0x73  | -70.0 | 0x48  | -91.5  | 0x1D  | -113.0 |
| 0xF3  | -6.0  | 0xC8  | -27.5 | 0x9D  | -49.0 | 0x72  | -70.5 | 0x47  | -92.0  | 0x1C  | -113.5 |
| 0xF2  | -6.5  | 0xC7  | -28.0 | 0x9C  | -49.5 | 0x71  | -71.0 | 0x46  | -92.5  | 0x1B  | -114.0 |
| 0xF1  | -7.0  | 0xC6  | -28.5 | 0x9B  | -50.0 | 0x70  | -71.5 | 0x45  | -93.0  | 0x1A  | -114.5 |
| 0xF0  | -7.5  | 0xC5  | -29.0 | 0x9A  | -50.5 | 0x6F  | -72.0 | 0x44  | -93.5  | 0x19  | -115.0 |
| 0xEF  | -8.0  | 0xC4  | -29.5 | 0x99  | -51.0 | 0x6E  | -72.5 | 0x43  | -94.0  | 0x18  | -115.5 |
| 0xEE  | -8.5  | 0xC3  | -30.0 | 0x98  | -51.5 | 0x6D  | -73.0 | 0x42  | -94.5  | 0x17  | -116.0 |
| 0xED  | -9.0  | 0xC2  | -30.5 | 0x97  | -52.0 | 0x6C  | -73.5 | 0x41  | -95.0  | 0x16  | -116.5 |
| 0xEC  | -9.5  | 0xC1  | -31.0 | 0x96  | -52.5 | 0x6B  | -74.0 | 0x40  | -95.5  | 0x15  | -117.0 |
| 0xEB  | -10.0 | 0xC0  | -31.5 | 0x95  | -53.0 | 0x6A  | -74.5 | 0x3F  | -96.0  | 0x14  | -117.5 |
| 0xEA  | -10.5 | 0xBF  | -32.0 | 0x94  | -53.5 | 0x69  | -75.0 | 0x3E  | -96.5  | 0x13  | -118.0 |
| 0xE9  | -11.0 | 0xBE  | -32.5 | 0x93  | -54.0 | 0x68  | -75.5 | 0x3D  | -97.0  | 0x12  | -118.5 |
| 0xE8  | -11.5 | 0xBD  | -33.0 | 0x92  | -54.5 | 0x67  | -76.0 | 0x3C  | -97.5  | 0x11  | -119.0 |
| 0xE7  | -12.0 | 0xBC  | -33.5 | 0x91  | -55.0 | 0x66  | -76.5 | 0x3B  | -98.0  | 0x10  | -119.5 |
| 0xE6  | -12.5 | 0xBB  | -34.0 | 0x90  | -55.5 | 0x65  | -77.0 | 0x3A  | -98.5  | 0x0F  | -120.0 |
| 0xE5  | -13.0 | 0xBA  | -34.5 | 0x8F  | -56.0 | 0x64  | -77.5 | 0x39  | -99.0  | 0x0E  | -120.5 |
| 0xE4  | -13.5 | 0xB9  | -35.0 | 0x8E  | -56.5 | 0x63  | -78.0 | 0x38  | -99.5  | 0x0D  | -121.0 |
| 0xE3  | -14.0 | 0xB8  | -35.5 | 0x8D  | -57.0 | 0x62  | -78.5 | 0x37  | -100.0 | 0x0C  | -121.5 |
| 0xE2  | -14.5 | 0xB7  | -36.0 | 0x8C  | -57.5 | 0x61  | -79.0 | 0x36  | -100.5 | 0x0B  | -122.0 |
| 0xE1  | -15.0 | 0xB6  | -36.5 | 0x8B  | -58.0 | 0x60  | -79.5 | 0x35  | -101.0 | 0x0A  | -122.5 |
| 0xE0  | -15.5 | 0xB5  | -37.0 | 0x8A  | -58.5 | 0x5F  | -80.0 | 0x34  | -101.5 | 0x09  | -123.0 |
| 0xDF  | -16.0 | 0xB4  | -37.5 | 0x89  | -59.0 | 0x5E  | -80.5 | 0x33  | -102.0 | 0x08  | -123.5 |
| 0xDE  | -16.5 | 0xB3  | -38.0 | 0x88  | -59.5 | 0x5D  | -81.0 | 0x32  | -102.5 | 0x07  | -124.0 |
| 0xDD  | -17.0 | 0xB2  | -38.5 | 0x87  | -60.0 | 0x5C  | -81.5 | 0x31  | -103.0 | 0x06  | -124.5 |
| 0xDC  | -17.5 | 0xB1  | -39.0 | 0x86  | -60.5 | 0x5B  | -82.0 | 0x30  | -103.5 | 0x05  | -125.0 |
| 0xDB  | -18.0 | 0xB0  | -39.5 | 0x85  | -61.0 | 0x5A  | -82.5 | 0x2F  | -104.0 | 0x04  | -125.5 |
| 0xDA  | -18.5 | 0xAF  | -40.0 | 0x84  | -61.5 | 0x59  | -83.0 | 0x2E  | -104.5 | 0x03  | NA     |
| 0xD9  | -19.0 | 0xAE  | -40.5 | 0x83  | -62.0 | 0x58  | -83.5 | 0x2D  | -105.0 | 0x02  | NA     |
| 0xD8  | -19.5 | 0xAD  | -41.0 | 0x82  | -62.5 | 0x57  | -84.0 | 0x2C  | -105.5 | 0x01  | NA     |
| 0xD7  | -20.0 | 0xAC  | -41.5 | 0x81  | -63.0 | 0x56  | -84.5 | 0x2B  | -106.0 | 0x00  | NA     |
| 0xD6  | -20.5 | 0xAB  | -42.0 | 0x80  | -63.5 | 0x55  | -85.0 | 0x2A  | -106.5 |       |        |
| 0xD5  | -21.0 | 0xAA  | -42.5 | 0x7F  | -64.0 | 0x54  | -85.5 | 0x29  | -107.0 |       |        |

Table 16. Channel Volume

| Index | dB   | Index | dB   | Index | dB    | Index | dB    | Index | dB    | Index | dB     |
|-------|------|-------|------|-------|-------|-------|-------|-------|-------|-------|--------|
| 0xFF  | 48.0 | 0xD4  | 26.5 | 0xA9  | 5.0   | 0x7E  | -16.5 | 0x53  | -38.0 | 0x28  | -59.5  |
| 0xFE  | 47.5 | 0xD3  | 26.0 | 0xA8  | 4.5   | 0x7D  | -17.0 | 0x52  | -38.5 | 0x27  | -60.0  |
| 0xFD  | 47.0 | 0xD2  | 25.5 | 0xA7  | 4.0   | 0x7C  | -17.5 | 0x51  | -39.0 | 0x26  | -60.5  |
| 0xFC  | 46.5 | 0xD1  | 25.0 | 0xA6  | 3.5   | 0x7B  | -18.0 | 0x50  | -39.5 | 0x25  | -61.0  |
| 0xFB  | 46.0 | 0xD0  | 24.5 | 0xA5  | 3.0   | 0x7A  | -18.5 | 0x4F  | -40.0 | 0x24  | -61.5  |
| 0xFA  | 45.5 | 0xCF  | 24.0 | 0xA4  | 2.5   | 0x79  | -19.0 | 0x4E  | -40.5 | 0x23  | -62.0  |
| 0xF9  | 45.0 | 0xCE  | 23.5 | 0xA3  | 2.0   | 0x78  | -19.5 | 0x4D  | -41.0 | 0x22  | -62.5  |
| 0xF8  | 44.5 | 0xCD  | 23.0 | 0xA2  | 1.5   | 0x77  | -20.0 | 0x4C  | -41.5 | 0x21  | -63.0  |
| 0xF7  | 44.0 | 0xCC  | 22.5 | 0xA1  | 1.0   | 0x76  | -20.5 | 0x4B  | -42.0 | 0x20  | -63.5  |
| 0xF6  | 43.5 | 0xCB  | 22.0 | 0xA0  | 0.5   | 0x75  | -21.0 | 0x4A  | -42.5 | 0x1F  | -64.0  |
| 0xF5  | 43.0 | 0xCA  | 21.5 | 0x9F  | 0.0   | 0x74  | -21.5 | 0x49  | -43.0 | 0x1E  | -64.5  |
| 0xF4  | 42.5 | 0xC9  | 21.0 | 0x9E  | -0.5  | 0x73  | -22.0 | 0x48  | -43.5 | 0x1D  | -65.0  |
| 0xF3  | 42.0 | 0xC8  | 20.5 | 0x9D  | -1.0  | 0x72  | -22.5 | 0x47  | -44.0 | 0x1C  | -65.5  |
| 0xF2  | 41.5 | 0xC7  | 20.0 | 0x9C  | -1.5  | 0x71  | -23.0 | 0x46  | -44.5 | 0x1B  | -66.0  |
| 0xF1  | 41.0 | 0xC6  | 19.5 | 0x9B  | -2.0  | 0x70  | -23.5 | 0x45  | -45.0 | 0x1A  | -66.5  |
| 0xF0  | 40.5 | 0xC5  | 19.0 | 0x9A  | -2.5  | 0x6F  | -24.0 | 0x44  | -45.5 | 0x19  | -67.0  |
| 0xEF  | 40.0 | 0xC4  | 18.5 | 0x99  | -3.0  | 0x6E  | -24.5 | 0x43  | -46.0 | 0x18  | -67.5  |
| 0xEE  | 39.5 | 0xC3  | 18.0 | 0x98  | -3.5  | 0x6D  | -25.0 | 0x42  | -46.5 | 0x17  | -68.0  |
| 0xED  | 39.0 | 0xC2  | 17.5 | 0x97  | -4.0  | 0x6C  | -25.5 | 0x41  | -47.0 | 0x16  | -68.5  |
| 0xEC  | 38.5 | 0xC1  | 17.0 | 0x96  | -4.5  | 0x6B  | -26.0 | 0x40  | -47.5 | 0x15  | -69.0  |
| 0xEB  | 38.0 | 0xC0  | 16.5 | 0x95  | -5.0  | 0x6A  | -26.5 | 0x3F  | -48.0 | 0x14  | -69.5  |
| 0xEA  | 37.5 | 0xBF  | 16.0 | 0x94  | -5.5  | 0x69  | -27.0 | 0x3E  | -48.5 | 0x13  | -70.0  |
| 0xE9  | 37.0 | 0xBE  | 15.5 | 0x93  | -6.0  | 0x68  | -27.5 | 0x3D  | -49.0 | 0x12  | -70.5  |
| 0xE8  | 36.5 | 0xBD  | 15.0 | 0x92  | -6.5  | 0x67  | -28.0 | 0x3C  | -49.5 | 0x11  | -71.0  |
| 0xE7  | 36.0 | 0xBC  | 14.5 | 0x91  | -7.0  | 0x66  | -28.5 | 0x3B  | -50.0 | 0x10  | -71.5  |
| 0xE6  | 35.5 | 0xBB  | 14.0 | 0x90  | -7.5  | 0x65  | -29.0 | 0x3A  | -50.5 | 0x0F  | -72.0  |
| 0xE5  | 35.0 | 0xBA  | 13.5 | 0x8F  | -8.0  | 0x64  | -29.5 | 0x39  | -51.0 | 0x0E  | -72.5  |
| 0xE4  | 34.5 | 0xB9  | 13.0 | 0x8E  | -8.5  | 0x63  | -30.0 | 0x38  | -51.5 | 0x0D  | -73.0  |
| 0xE3  | 34.0 | 0xB8  | 12.5 | 0x8D  | -9.0  | 0x62  | -30.5 | 0x37  | -52.0 | 0x0C  | -73.5  |
| 0xE2  | 33.5 | 0xB7  | 12.0 | 0x8C  | -9.5  | 0x61  | -31.0 | 0x36  | -52.5 | 0x0B  | -74.0  |
| 0xE1  | 33.0 | 0xB6  | 11.5 | 0x8B  | -10.0 | 0x60  | -31.5 | 0x35  | -53.0 | 0x0A  | -74.5  |
| 0xE0  | 32.5 | 0xB5  | 11.0 | 0x8A  | -10.5 | 0x5F  | -32.0 | 0x34  | -53.5 | 0x09  | -75.0  |
| 0xDF  | 32.0 | 0xB4  | 10.5 | 0x89  | -11.0 | 0x5E  | -32.5 | 0x33  | -54.0 | 0x08  | -75.5  |
| 0xDE  | 31.5 | 0xB3  | 10.0 | 0x88  | -11.5 | 0x5D  | -33.0 | 0x32  | -54.5 | 0x07  | -76.0  |
| 0xDD  | 31.0 | 0xB2  | 9.5  | 0x87  | -12.0 | 0x5C  | -33.5 | 0x31  | -55.0 | 0x06  | -76.5  |
| 0xDC  | 30.5 | 0xB1  | 9.0  | 0x86  | -12.5 | 0x5B  | -34.0 | 0x30  | -55.5 | 0x05  | -77.0  |
| 0xDB  | 30.0 | 0xB0  | 8.5  | 0x85  | -13.0 | 0x5A  | -34.5 | 0x2F  | -56.0 | 0x04  | -77.5  |
| 0xDA  | 29.5 | 0xAF  | 8.0  | 0x84  | -13.5 | 0x59  | -35.0 | 0x2E  | -56.5 | 0x03  | -78.0  |
| 0xD9  | 29.0 | 0xAE  | 7.5  | 0x83  | -14.0 | 0x58  | -35.5 | 0x2D  | -57.0 | 0x02  | -78.5  |
| 0xD8  | 28.5 | 0xAD  | 7.0  | 0x82  | -14.5 | 0x57  | -36.0 | 0x2C  | -57.5 | 0x01  | -79.0  |
| 0xD7  | 28.0 | 0xAC  | 6.5  | 0x81  | -15.0 | 0x56  | -36.5 | 0x2B  | -58.0 | 0x00  | -295.0 |
| 0xD6  | 27.5 | 0xAB  | 6.0  | 0x80  | -15.5 | 0x55  | -37.0 | 0x2A  | -58.5 |       |        |
| 0xD5  | 27.0 | 0xAA  | 5.5  | 0x7F  | -16.0 | 0x54  | -37.5 | 0x29  | -59.0 |       |        |

Table 17. Mixer Gain & Polarity

| Index | Polarity | dB   | Index | Polarity | dB   | Index | Polarity | dB   | Index | Polarity | dB   |
|-------|----------|------|-------|----------|------|-------|----------|------|-------|----------|------|
| 7E    | +        | 18   | 7D    | -        | 18   | 3E    | +        | -4   | 3D    | -        | -4   |
| 7C    | +        | 17   | 7B    | -        | 17   | 3C    | +        | -4.5 | 3B    | -        | -4.5 |
| 7A    | +        | 16   | 79    | -        | 16   | 3A    | +        | -5   | 39    | -        | -5   |
| 78    | +        | 15   | 77    | -        | 15   | 38    | +        | -5.5 | 37    | -        | -5.5 |
| 76    | +        | 14   | 75    | -        | 14   | 36    | +        | -6   | 35    | -        | -6   |
| 74    | +        | 13   | 73    | -        | 13   | 34    | +        | -7   | 33    | -        | -7   |
| 72    | +        | 12   | 71    | -        | 12   | 32    | +        | -8   | 31    | -        | -8   |
| 70    | +        | 11   | 6F    | -        | 11   | 30    | +        | -9   | 2F    | -        | -9   |
| 6E    | +        | 10   | 6D    | -        | 10   | 2E    | +        | -10  | 2D    | -        | -10  |
| 6C    | +        | 9    | 6B    | -        | 9    | 2C    | +        | -11  | 2B    | -        | -11  |
| 6A    | +        | 8    | 69    | -        | 8    | 2A    | +        | -12  | 29    | -        | -12  |
| 68    | +        | 7    | 67    | -        | 7    | 28    | +        | -13  | 27    | -        | -13  |
| 66    | +        | 6    | 65    | -        | 6    | 26    | +        | -14  | 25    | -        | -14  |
| 64    | +        | 5.5  | 63    | -        | 5.5  | 24    | +        | -15  | 23    | -        | -15  |
| 62    | +        | 5    | 61    | -        | 5    | 22    | +        | -16  | 21    | -        | -16  |
| 60    | +        | 4.5  | 5F    | -        | 4.5  | 20    | +        | -17  | 1F    | -        | -17  |
| 5E    | +        | 4    | 5D    | -        | 4    | 1E    | +        | -18  | 1D    | -        | -18  |
| 5C    | +        | 3.5  | 5B    | -        | 3.5  | 1C    | +        | -19  | 1B    | -        | -19  |
| 5A    | +        | 3    | 59    | -        | 3    | 1A    | +        | -20  | 19    | -        | -20  |
| 58    | +        | 2.5  | 57    | -        | 2.5  | 18    | +        | -21  | 17    | -        | -21  |
| 56    | +        | 2    | 55    | -        | 2    | 16    | +        | -22  | 15    | -        | -22  |
| 54    | +        | 1.5  | 53    | -        | 1.5  | 14    | +        | -23  | 13    | -        | -23  |
| 52    | +        | 1    | 51    | -        | 1    | 12    | +        | -24  | 11    | -        | -24  |
| 50    | +        | 0.5  | 4F    | -        | 0.5  | 10    | +        | -25  | 0F    | -        | -25  |
| 4E    | +        | 0    | 4D    | -        | 0    | 0E    | +        | -26  | 0D    | -        | -26  |
| 4C    | +        | -0.5 | 4B    | -        | -0.5 | 0C    | +        | -27  | 0B    | -        | -27  |
| 4A    | +        | -1   | 49    | -        | -1   | 0A    | +        | -28  | 09    | -        | -28  |
| 48    | +        | -1.5 | 47    | -        | -1.5 | 08    | +        | -29  | 07    | -        | -29  |
| 46    | +        | -2   | 45    | -        | -2   | 06    | +        | -30  | 05    | -        | -30  |
| 44    | +        | -2.5 | 43    | -        | -2.5 | 04    | +        | -31  | 03    | -        | -31  |
| 42    | +        | -3   | 41    | -        | -3   | 02    | +        | -32  | 01    | -        | -32  |
| 40    | +        | -3.5 | 3F    | -        | -3.5 | 00    | +        | -150 |       |          |      |

Table 18. Dynamic Range Control Threshold

| dB    | Value | dB   | Value | dB   | Value | dB   | Value |
|-------|-------|------|-------|------|-------|------|-------|
| -57   | FF    | -5.5 | DF    | -2.3 | BF    | 0.9  | 9F    |
| -54   | FE    | -5.4 | DE    | -2.2 | BE    | 1    | 9E    |
| -51   | FD    | -5.3 | DD    | -2.1 | BD    | 1.25 | 9D    |
| -48   | FC    | -5.2 | DC    | -2   | BC    | 1.5  | 9C    |
| -45   | FB    | -5.1 | DB    | -1.9 | BB    | 1.75 | 9B    |
| -42   | FA    | -5   | DA    | -1.8 | BA    | 2    | 9A    |
| -39   | F9    | -4.9 | D9    | -1.7 | B9    | 2.25 | 99    |
| -36   | F8    | -4.8 | D8    | -1.6 | B8    | 2.5  | 98    |
| -33   | F7    | -4.7 | D7    | -1.5 | B7    | 2.75 | 97    |
| -30   | F6    | -4.6 | D6    | -1.4 | B6    | 3    | 96    |
| -27   | F5    | -4.5 | D5    | -1.3 | B5    | 3.25 | 95    |
| -24   | F4    | -4.4 | D4    | -1.2 | B4    | 3.5  | 94    |
| -21   | F3    | -4.3 | D3    | -1.1 | B3    | 3.75 | 93    |
| -18   | F2    | -4.2 | D2    | -1   | B2    | 4    | 92    |
| -15   | F1    | -4.1 | D1    | -0.9 | B1    | 4.25 | 91    |
| -12   | F0    | -4   | D0    | -0.8 | B0    | 4.5  | 90    |
| -11.5 | EF    | -3.9 | CF    | -0.7 | AF    | 4.75 | 8F    |
| -11   | EE    | -3.8 | CE    | -0.6 | AE    | 5    | 8E    |
| -10.5 | ED    | -3.7 | CD    | -0.5 | AD    | 5.5  | 8D    |
| -10   | EC    | -3.6 | CC    | -0.4 | AC    | 6    | 8C    |
| -9.5  | EB    | -3.5 | CB    | -0.3 | AB    | 6.5  | 8B    |
| -9    | EA    | -3.4 | CA    | -0.2 | AA    | 7    | 8A    |
| -8.5  | E9    | -3.3 | C9    | -0.1 | A9    | 7.5  | 89    |
| -8    | E8    | -3.2 | C8    | 0    | A8    | 8    | 88    |
| -7.5  | E7    | -3.1 | C7    | 0.1  | A7    | 8.5  | 87    |
| -7    | E6    | -3   | C6    | 0.2  | A6    | 9    | 86    |
| -6.5  | E5    | -2.9 | C5    | 0.3  | A5    | 9.5  | 85    |
| -6    | E4    | -2.8 | C4    | 0.4  | A4    | 10   | 84    |
| -5.9  | E3    | -2.7 | C3    | 0.5  | A3    | 10.5 | 83    |
| -5.8  | E2    | -2.6 | C2    | 0.6  | A2    | 11   | 82    |
| -5.7  | E1    | -2.5 | C1    | 0.7  | A1    | 11.5 | 81    |
| -5.6  | E0    | -2.4 | C0    | 0.8  | A0    | 12   | 80    |

※ CPR bit(MSB) = 1



**Table 19. Auto Mute Detection Threshold Table**

| Name | Description                         | Value       | dB               |
|------|-------------------------------------|-------------|------------------|
| AT   | Auto-mute<br>Detection<br>threshold | 0000        | -126             |
|      |                                     | 0001        | -120             |
|      |                                     | 0010        | -114             |
|      |                                     | 0011        | -108             |
|      |                                     | 0100        | -102             |
|      |                                     | 0101        | -96              |
|      |                                     | 0110        | -90              |
|      |                                     | 0111        | -84              |
|      |                                     | 1000        | -78              |
|      |                                     | 1001        | -72              |
|      |                                     | 1010        | -66              |
|      |                                     | 1011        | -60              |
|      |                                     | 1100        | -54              |
|      |                                     | 1101        | -48              |
|      |                                     | 1110        | -42              |
|      |                                     | <b>1111</b> | <b>Auto-mute</b> |

※ Do not use value 1111.

CONFIDENTIAL

**Table 20. Power Meter Reading Table**

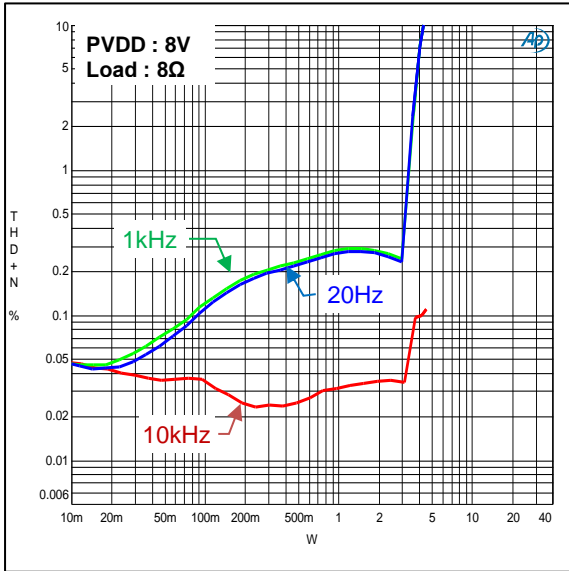
| addr 0x54 (Decimal) | addr 0x54 (Hex) | dB    | addr 0x54 (Decimal) | addr 0x54 (Hex) | dB    | addr 0x54 (Decimal) | addr 0x54 (Hex) | dB    | addr 0x54 (Decimal) | addr 0x54 (Hex) | dB           |
|---------------------|-----------------|-------|---------------------|-----------------|-------|---------------------|-----------------|-------|---------------------|-----------------|--------------|
| 0                   | 0x00            | -0.0  | 64                  | 0x40            | -32.0 | 128                 | 0x80            | -64.0 | 192                 | 0xC0            | -96.0        |
| 1                   | 0x01            | -0.5  | 65                  | 0x41            | -32.5 | 129                 | 0x81            | -64.5 | 193                 | 0xC1            | -96.5        |
| 2                   | 0x02            | -1.0  | 66                  | 0x42            | -33.0 | 130                 | 0x82            | -65.0 | 194                 | 0xC2            | -97.0        |
| 3                   | 0x03            | -1.5  | 67                  | 0x43            | -33.5 | 131                 | 0x83            | -65.5 | 195                 | 0xC3            | -97.5        |
| 4                   | 0x04            | -2.0  | 68                  | 0x44            | -34.0 | 132                 | 0x84            | -66.0 | 196                 | 0xC4            | -98.0        |
| 5                   | 0x05            | -2.5  | 69                  | 0x45            | -34.5 | 133                 | 0x85            | -66.5 | 197                 | 0xC5            | -98.5        |
| 6                   | 0x06            | -3.0  | 70                  | 0x46            | -35.0 | 134                 | 0x86            | -67.0 | 198                 | 0xC6            | -99.0        |
| 7                   | 0x07            | -3.5  | 71                  | 0x47            | -35.5 | 135                 | 0x87            | -67.5 | 199                 | 0xC7            | -99.5        |
| 8                   | 0x08            | -4.0  | 72                  | 0x48            | -36.0 | 136                 | 0x88            | -68.0 | 200                 | 0xC8            | -100.0       |
| 9                   | 0x09            | -4.5  | 73                  | 0x49            | -36.5 | 137                 | 0x89            | -68.5 | 201                 | 0xC9            | -100.5       |
| 10                  | 0x0A            | -5.0  | 74                  | 0x4A            | -37.0 | 138                 | 0x8A            | -69.0 | 202                 | 0xCA            | -101.0       |
| 11                  | 0x0B            | -5.5  | 75                  | 0x4B            | -37.5 | 139                 | 0x8B            | -69.5 | 203                 | 0xCB            | -101.5       |
| 12                  | 0x0C            | -6.0  | 76                  | 0x4C            | -38.0 | 140                 | 0x8C            | -70.0 | 204                 | 0xCC            | -102.0       |
| 13                  | 0x0D            | -6.5  | 77                  | 0x4D            | -38.5 | 141                 | 0x8D            | -70.5 | 205                 | 0xCD            | -102.5       |
| 14                  | 0x0E            | -7.0  | 78                  | 0x4E            | -39.0 | 142                 | 0x8E            | -71.0 | 206                 | 0xCE            | -103.0       |
| 15                  | 0x0F            | -7.5  | 79                  | 0x4F            | -39.5 | 143                 | 0x8F            | -71.5 | 207                 | 0xCF            | -103.5       |
| 16                  | 0x10            | -8.0  | 80                  | 0x50            | -40.0 | 144                 | 0x90            | -72.0 | 208                 | 0xD0            | -104.0       |
| 17                  | 0x11            | -8.5  | 81                  | 0x51            | -40.5 | 145                 | 0x91            | -72.5 | 209                 | 0xD1            | -104.5       |
| 18                  | 0x12            | -9.0  | 82                  | 0x52            | -41.0 | 146                 | 0x92            | -73.0 | 210                 | 0xD2            | -105.0       |
| 19                  | 0x13            | -9.5  | 83                  | 0x53            | -41.5 | 147                 | 0x93            | -73.5 | 211                 | 0xD3            | -105.5       |
| 20                  | 0x14            | -10.0 | 84                  | 0x54            | -42.0 | 148                 | 0x94            | -74.0 | 212                 | 0xD4            | -106.0       |
| 21                  | 0x15            | -10.5 | 85                  | 0x55            | -42.5 | 149                 | 0x95            | -74.5 | 213                 | 0xD5            | -106.5       |
| 22                  | 0x16            | -11.0 | 86                  | 0x56            | -43.0 | 150                 | 0x96            | -75.0 | 214                 | 0xD6            | -107.0       |
| 23                  | 0x17            | -11.5 | 87                  | 0x57            | -43.5 | 151                 | 0x97            | -75.5 | 215                 | 0xD7            | -107.5       |
| 24                  | 0x18            | -12.0 | 88                  | 0x58            | -44.0 | 152                 | 0x98            | -76.0 | 216                 | 0xD8            | -108.0       |
| 25                  | 0x19            | -12.5 | 89                  | 0x59            | -44.5 | 153                 | 0x99            | -76.5 | 217                 | 0xD9            | -108.5       |
| 26                  | 0x1A            | -13.0 | 90                  | 0x5A            | -45.0 | 154                 | 0x9A            | -77.0 | 218                 | 0xDA            | -109.0       |
| 27                  | 0x1B            | -13.5 | 91                  | 0x5B            | -45.5 | 155                 | 0x9B            | -77.5 | 219                 | 0xDB            | -109.5       |
| 28                  | 0x1C            | -14.0 | 92                  | 0x5C            | -46.0 | 156                 | 0x9C            | -78.0 | 220                 | 0xDC            | -110.0       |
| 29                  | 0x1D            | -14.5 | 93                  | 0x5D            | -46.5 | 157                 | 0x9D            | -78.5 | 221                 | 0xDD            | -110.5       |
| 30                  | 0x1E            | -15.0 | 94                  | 0x5E            | -47.0 | 158                 | 0x9E            | -79.0 | 222                 | 0xDE            | -111.0       |
| 31                  | 0x1F            | -15.5 | 95                  | 0x5F            | -47.5 | 159                 | 0x9F            | -79.5 | 223                 | 0xDF            | -111.5       |
| 32                  | 0x20            | -16.0 | 96                  | 0x60            | -48.0 | 160                 | 0xA0            | -80.0 | 224                 | 0xE0            | -112.0       |
| 33                  | 0x21            | -16.5 | 97                  | 0x61            | -48.5 | 161                 | 0xA1            | -80.5 | 225                 | 0xE1            | -112.5       |
| 34                  | 0x22            | -17.0 | 98                  | 0x62            | -49.0 | 162                 | 0xA2            | -81.0 | 226                 | 0xE2            | -113.0       |
| 35                  | 0x23            | -17.5 | 99                  | 0x63            | -49.5 | 163                 | 0xA3            | -81.5 | 227                 | 0xE3            | -113.5       |
| 36                  | 0x24            | -18.0 | 100                 | 0x64            | -50.0 | 164                 | 0xA4            | -82.0 | 228                 | 0xE4            | -114.0       |
| 37                  | 0x25            | -18.5 | 101                 | 0x65            | -50.5 | 165                 | 0xA5            | -82.5 | 229                 | 0xE5            | -114.5       |
| 38                  | 0x26            | -19.0 | 102                 | 0x66            | -51.0 | 166                 | 0xA6            | -83.0 | 230                 | 0xE6            | -115.0       |
| 39                  | 0x27            | -19.5 | 103                 | 0x67            | -51.5 | 167                 | 0xA7            | -83.5 | 231                 | 0xE7            | -115.5       |
| 40                  | 0x28            | -20.0 | 104                 | 0x68            | -52.0 | 168                 | 0xA8            | -84.0 | 232                 | 0xE8            | -116.0       |
| 41                  | 0x29            | -20.5 | 105                 | 0x69            | -52.5 | 169                 | 0xA9            | -84.5 | 233                 | 0xE9            | -116.5       |
| 42                  | 0x2A            | -21.0 | 106                 | 0x6A            | -53.0 | 170                 | 0xAA            | -85.0 | 234                 | 0xEA            | -117.0       |
| 43                  | 0x2B            | -21.5 | 107                 | 0x6B            | -53.5 | 171                 | 0xAB            | -85.5 | 235                 | 0xEB            | -117.5       |
| 44                  | 0x2C            | -22.0 | 108                 | 0x6C            | -54.0 | 172                 | 0xAC            | -86.0 | 236                 | 0xEC            | -118.0       |
| 45                  | 0x2D            | -22.5 | 109                 | 0x6D            | -54.5 | 173                 | 0xAD            | -86.5 | 237                 | 0xED            | -118.5       |
| 46                  | 0x2E            | -23.0 | 110                 | 0x6E            | -55.0 | 174                 | 0xAE            | -87.0 | 238                 | 0xEE            | -119.0       |
| 47                  | 0x2F            | -23.5 | 111                 | 0x6F            | -55.5 | 175                 | 0xAF            | -87.5 | 239                 | 0xEF            | -119.5       |
| 48                  | 0x30            | -24.0 | 112                 | 0x70            | -56.0 | 176                 | 0xB0            | -88.0 | 240                 | 0xF0            | -120.0       |
| 49                  | 0x31            | -24.5 | 113                 | 0x71            | -56.5 | 177                 | 0xB1            | -88.5 | 241                 | 0xF1            | -120.5       |
| 50                  | 0x32            | -25.0 | 114                 | 0x72            | -57.0 | 178                 | 0xB2            | -89.0 | 242                 | 0xF2            | -121.0       |
| 51                  | 0x33            | -25.5 | 115                 | 0x73            | -57.5 | 179                 | 0xB3            | -89.5 | 243                 | 0xF3            | -121.5       |
| 52                  | 0x34            | -26.0 | 116                 | 0x74            | -58.0 | 180                 | 0xB4            | -90.0 | 244                 | 0xF4            | -122.0       |
| 53                  | 0x35            | -26.5 | 117                 | 0x75            | -58.5 | 181                 | 0xB5            | -90.5 | 245                 | 0xF5            | -122.5       |
| 54                  | 0x36            | -27.0 | 118                 | 0x76            | -59.0 | 182                 | 0xB6            | -91.0 | 246                 | 0xF6            | -123.0       |
| 55                  | 0x37            | -27.5 | 119                 | 0x77            | -59.5 | 183                 | 0xB7            | -91.5 | 247                 | 0xF7            | -123.5       |
| 56                  | 0x38            | -28.0 | 120                 | 0x78            | -60.0 | 184                 | 0xB8            | -92.0 | 248                 | 0xF8            | -124.0       |
| 57                  | 0x39            | -28.5 | 121                 | 0x79            | -60.5 | 185                 | 0xB9            | -92.5 | 249                 | 0xF9            | -124.5       |
| 58                  | 0x3A            | -29.0 | 122                 | 0x7A            | -61.0 | 186                 | 0xBA            | -93.0 | 250                 | 0xFA            | -125.0       |
| 59                  | 0x3B            | -29.5 | 123                 | 0x7B            | -61.5 | 187                 | 0xBB            | -93.5 | 251                 | 0xFB            | -125.5       |
| 60                  | 0x3C            | -30.0 | 124                 | 0x7C            | -62.0 | 188                 | 0xBC            | -94.0 | 252                 | 0xFC            | -126.0       |
| 61                  | 0x3D            | -30.5 | 125                 | 0x7D            | -62.5 | 189                 | 0xBD            | -94.5 | 253                 | 0xFD            | -126.5       |
| 62                  | 0x3E            | -31.0 | 126                 | 0x7E            | -63.0 | 190                 | 0xBE            | -95.0 | 254                 | 0xFE            | -127.0       |
| 63                  | 0x3F            | -31.5 | 127                 | 0x7F            | -63.5 | 191                 | 0xBF            | -95.5 | 255                 | 0xFF            | -127.5 under |

※ Output 8bit value :  $(-dB * 2)$ , n dB = output 8bit \*0.5

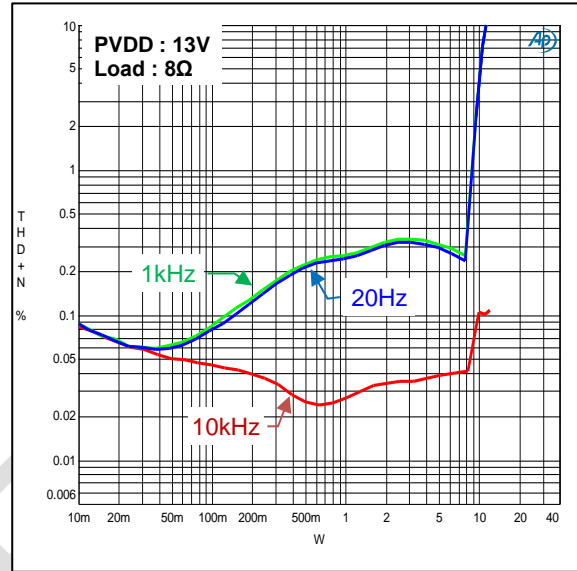
### C. Typical Characteristics Graph

#### Total Harmonic Distortion + Noise vs. Power, BTL D-BTL Mode Configuration, 8Ω

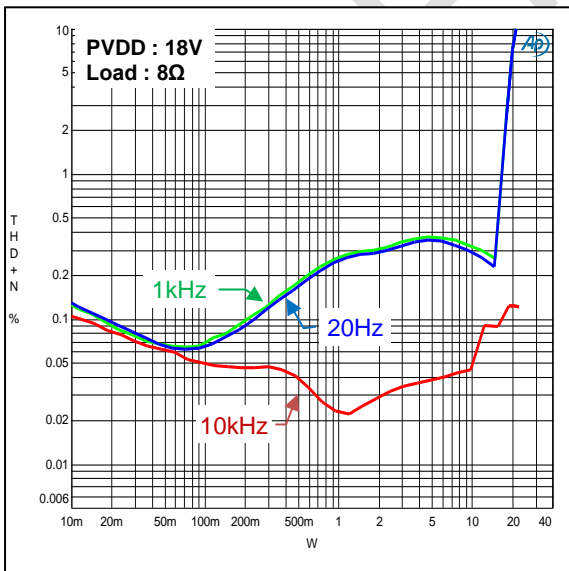
THD+N vs. Power



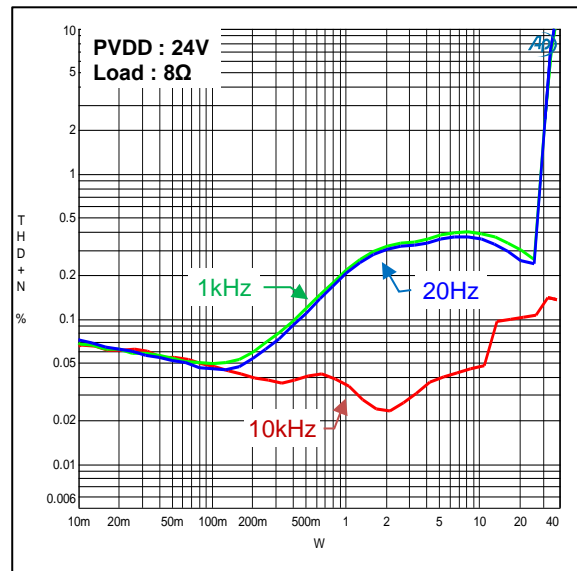
THD+N vs. Power



THD+N vs. Power

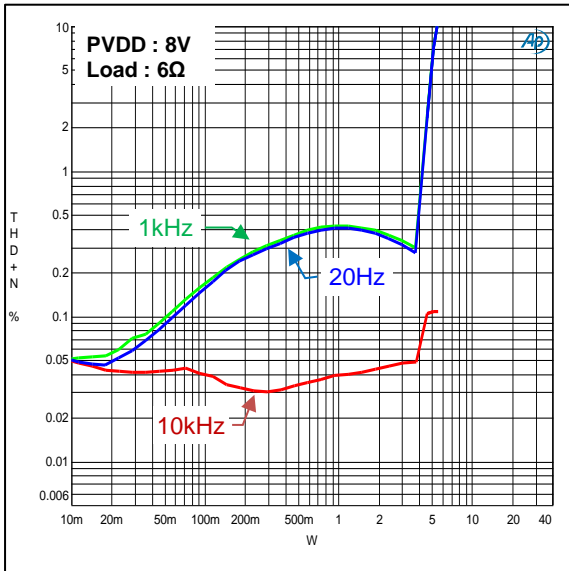


THD+N vs. Power

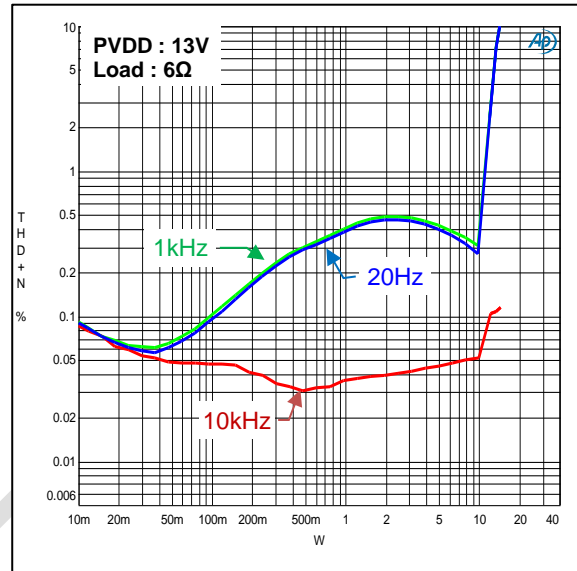


**Total Harmonic Distortion + Noise vs. Power, BTL D-BTL Mode Configuration, 6Ω**

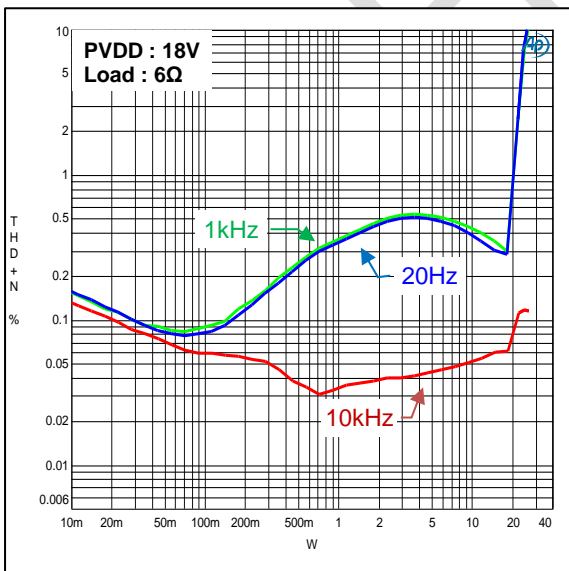
**THD+N vs. Power**



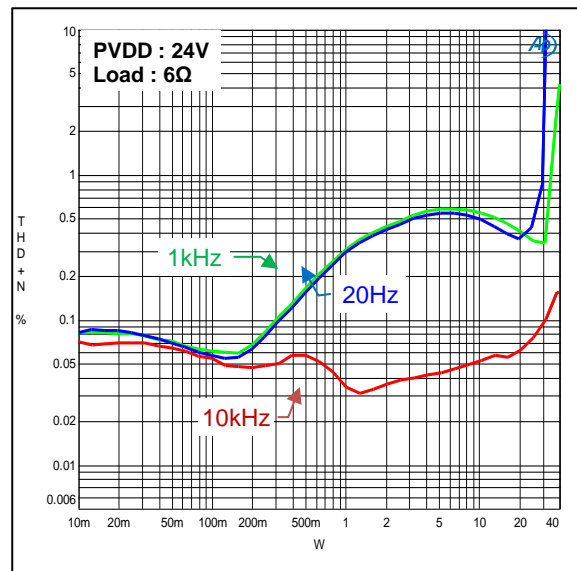
**THD+N vs. Power**



**THD+N vs. Power**

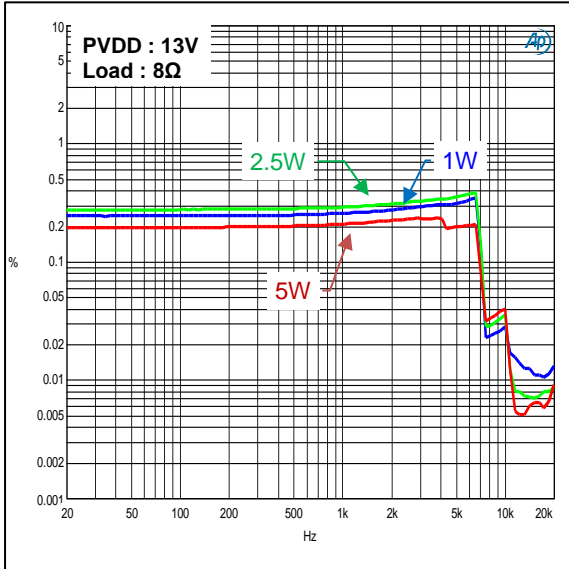


**THD+N vs. Power**

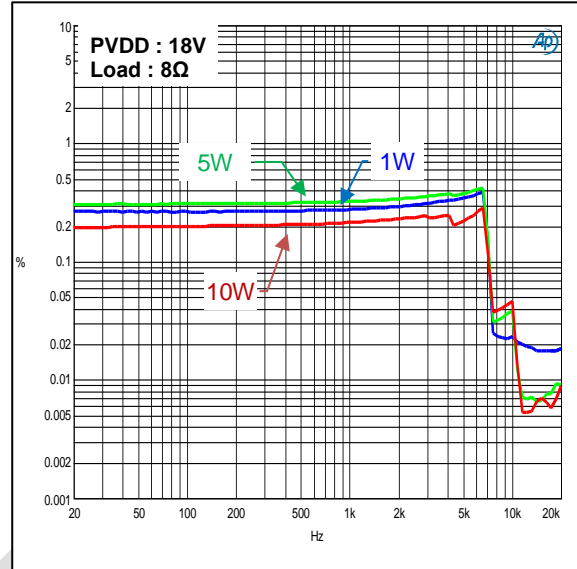


**Total Harmonic Distortion + Noise vs. Frequency, BTL D-BTL Mode Configuration, 8Ω**

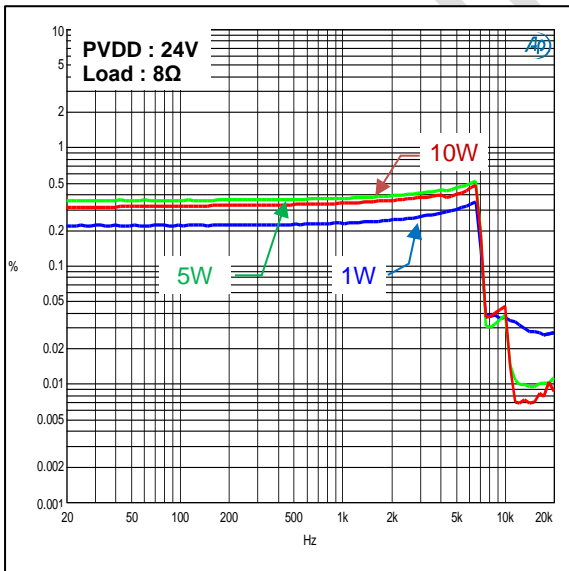
**THD+N vs. Frequency**



**THD+N vs. Frequency**

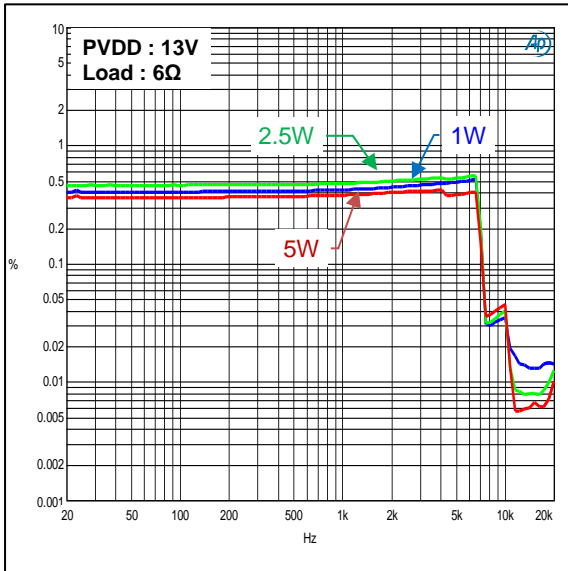


**THD+N vs. Frequency**

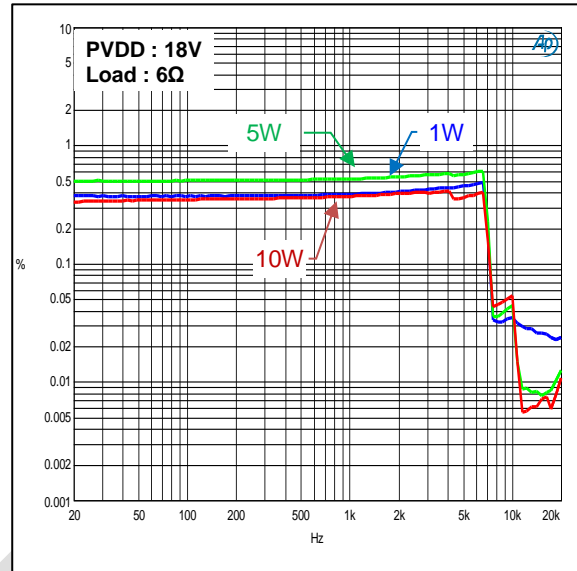


Total Harmonic Distortion + Noise vs. Frequency, BTL D-BTL Mode Configuration, 6Ω

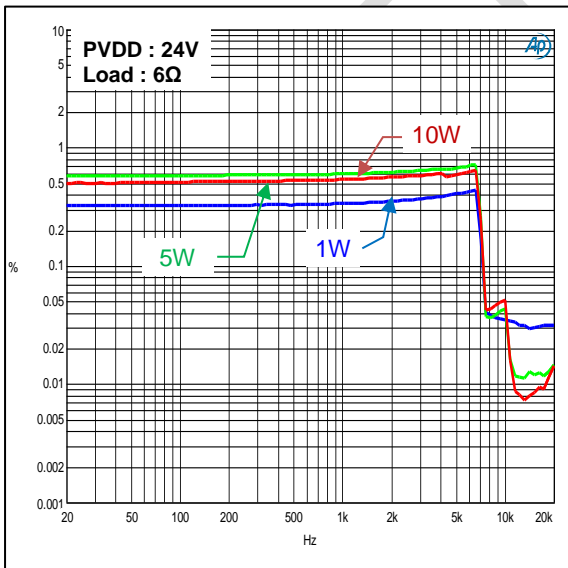
THD+N vs. Frequency



THD+N vs. Frequency

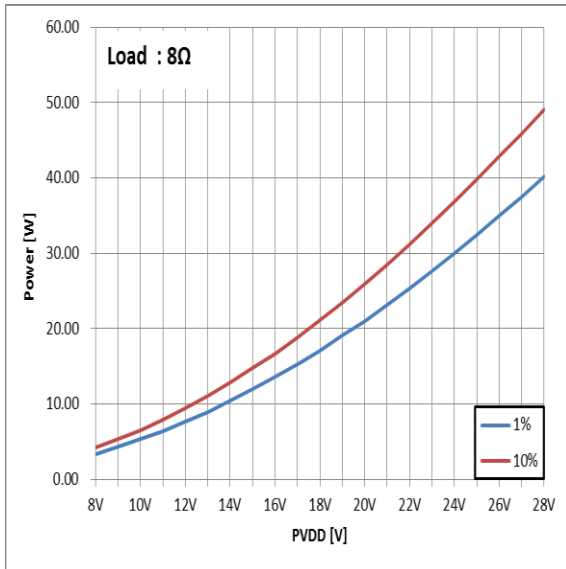


THD+N vs. Frequency

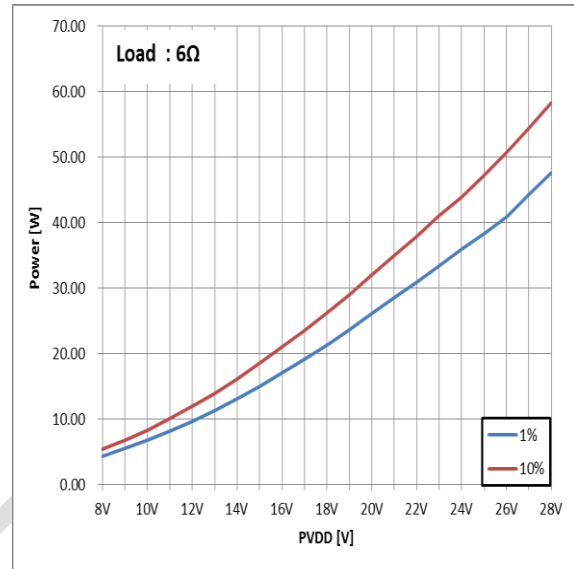


Output Power vs. PVDD, BTL D-BTL Mode Configuration

Output Power vs. PVDD

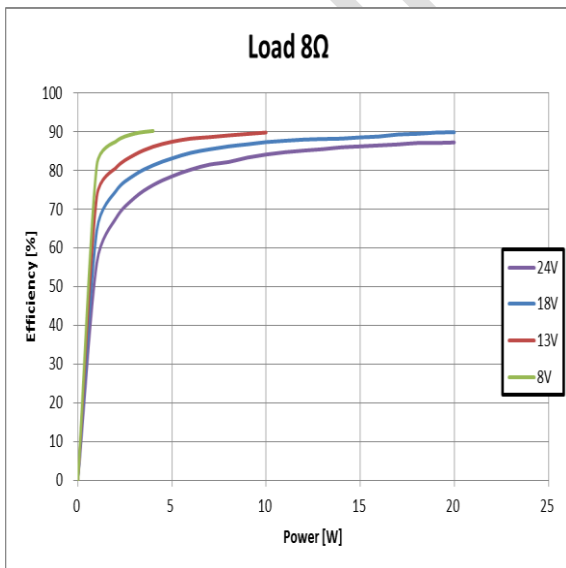


Output Power vs. PVDD

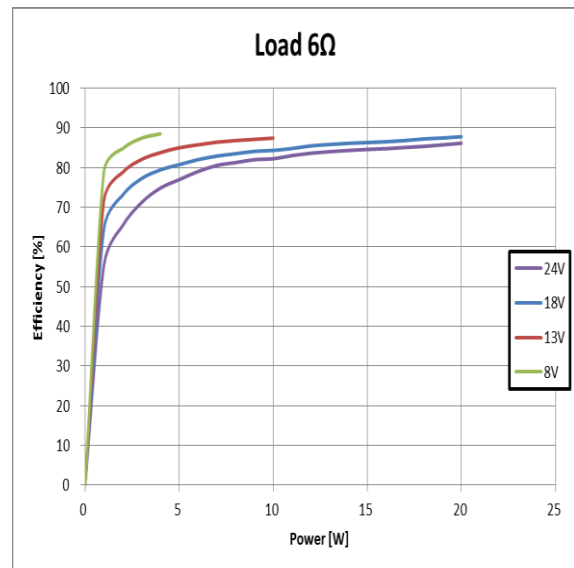


Efficiency vs. Total Power, BTL D-BTL Mode Configuration

Efficiency vs. Output Power

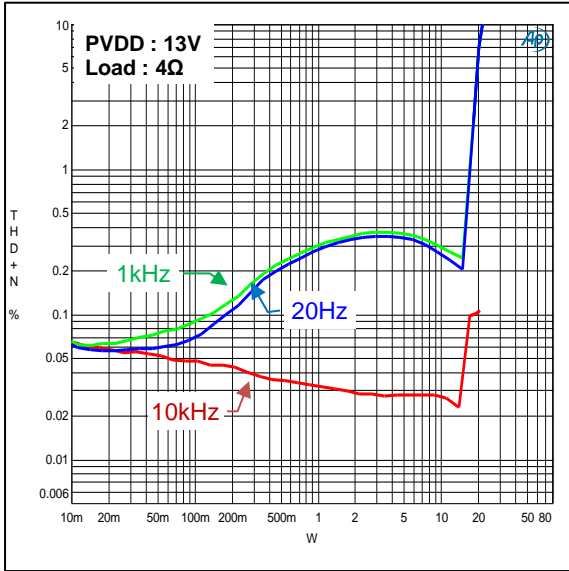


Efficiency vs. Output Power

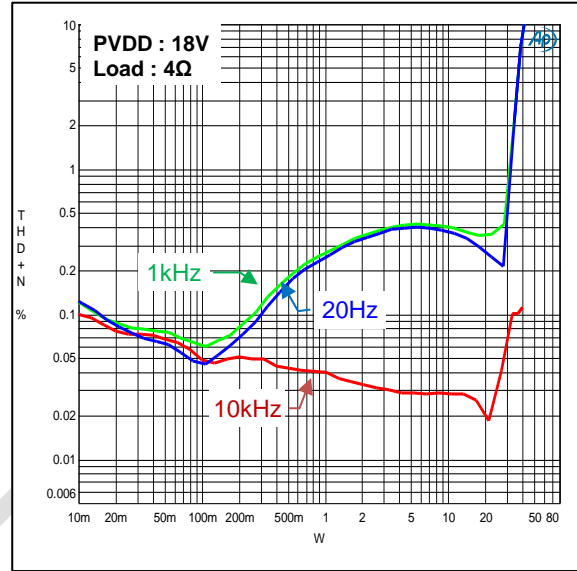


**Total Harmonic Distortion + Noise vs. Power, PBTL AD Mode Configuration, 4Ω**

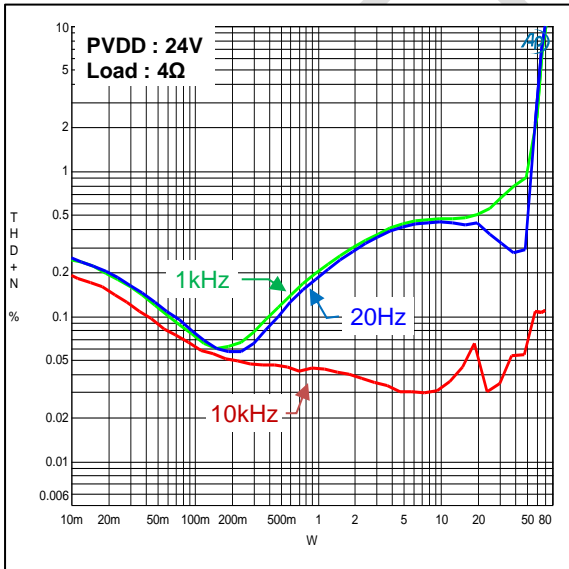
**THD+N vs. Power**



**THD+N vs. Power**



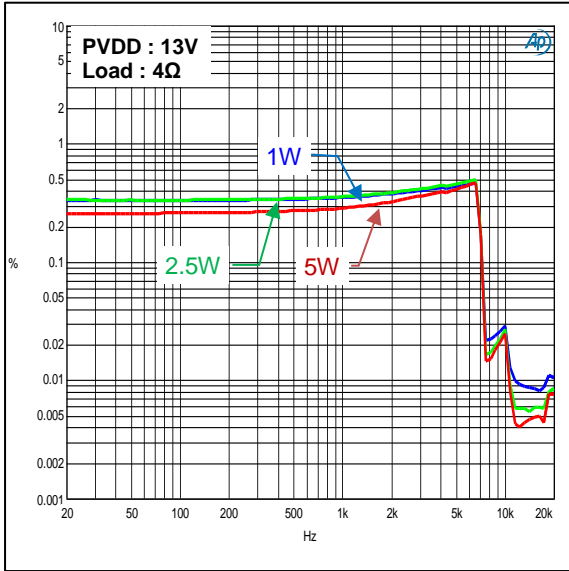
**THD+N vs. Power**



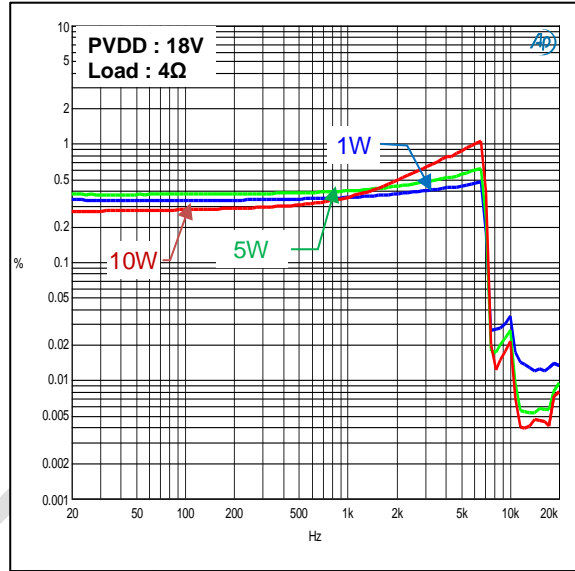


Total Harmonic Distortion + Noise vs. Frequency, PBTL AD Mode Configuration, 4Ω

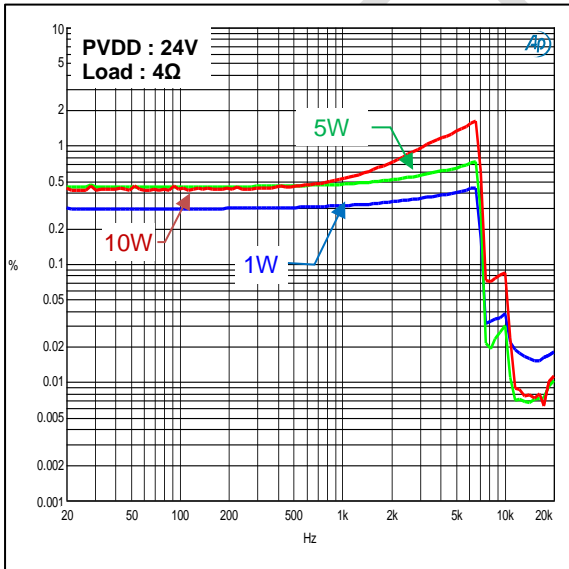
THD+N vs. Frequency



THD+N vs. Frequency

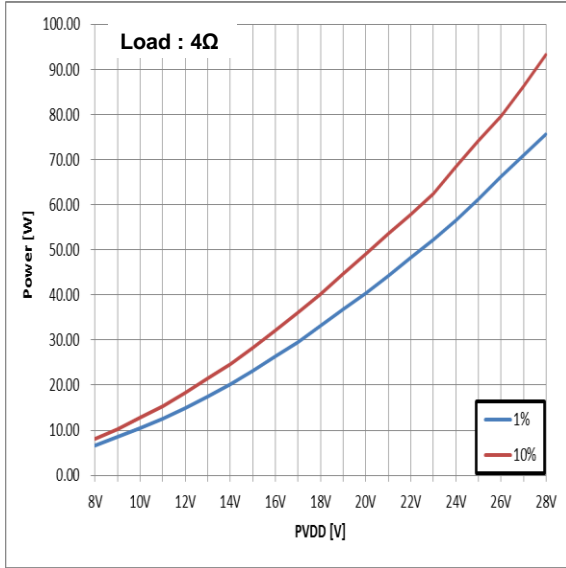


THD+N vs. Frequency



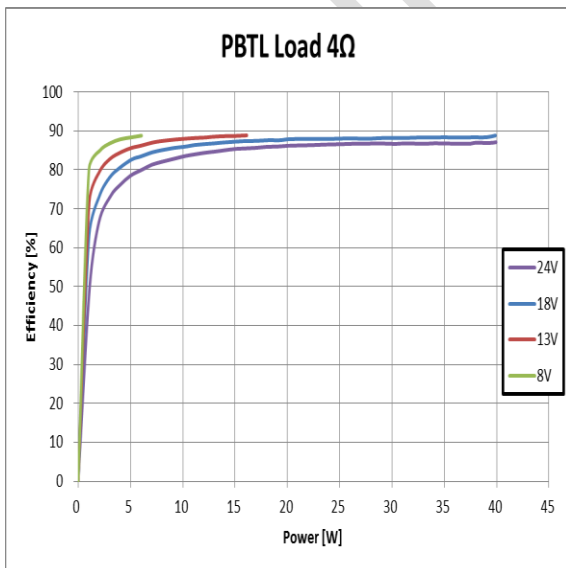
Output Power vs. PVDD, PBTL AD Mode Configuration

Output Power vs. PVDD

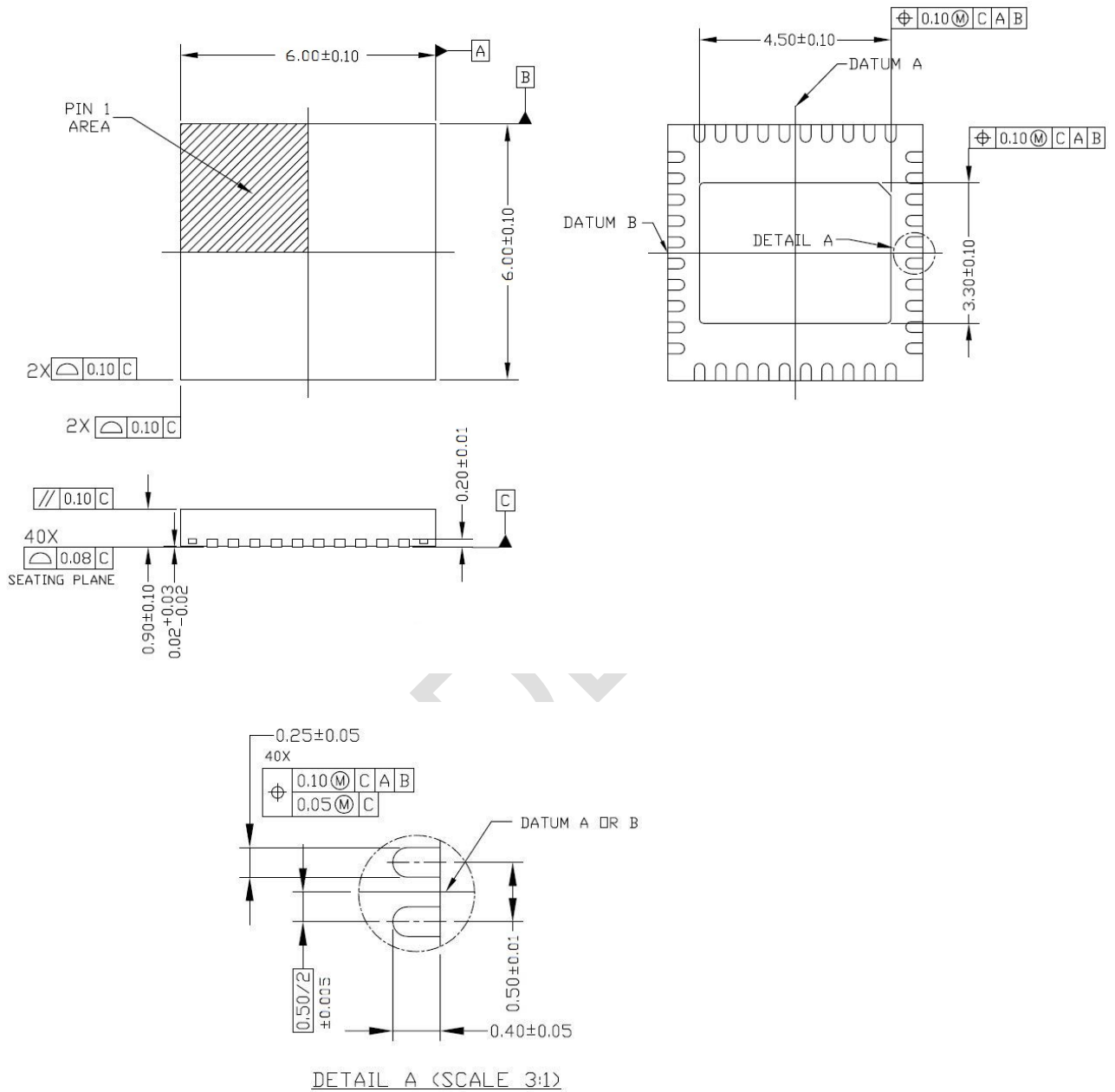


Efficiency vs. Total Power, PBTL AD Mode Configuration

Efficiency vs. Output Power



### D. Outline and Mechanical Data



NOTES:

- DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994.  
ALL DIMENSIONS ARE IN MILLIMETERS \* IN DEGREES
- DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA