

# KEROSLite<sup>®</sup>

## KERBEROS Lite OTP

Data Sheet Version 0.0

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Revision History

Doc. Rev.	Date	Comments
KEROSLite_v0.0	11/15/2017	Initial document release

1 Introduction

The KEROS-Lite is a family of high performance 64Bytes OTP memory with advanced built-in AES 256 security engine and cryptographic features

Through dynamic, symmetric mutual authentication, data encryption and the use of data decryption provides a secure place for storage of sensitive information within a system. With its protection circuit, this information remains safely even under attack.

The KEROS-Lite also provides high security, low cost and easy implementation of host-client type systems without the needs for a MCU operating system. The embedded AES256 cryptographic engine provides for a dynamic, symmetric mutual authentication between the device and host, as well as performs encryption for all data and passwords exchanged between the device and host. The AES256 unique key set may be used for these operations.

The simplified host library providing to customers and customers can access easily to deal with the KEROS-Lite

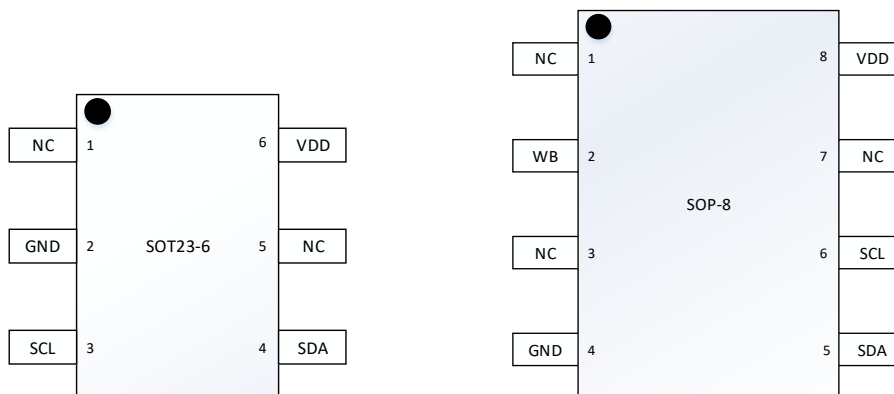


Figure [1.1] available package of KEROS-Lite (Top view)

## 1.1 Features

- High security features
  - Symmetric-mutual authentication
  - AES 256 bits encryption and decryption engine
  - I2C protocol with random stream encryption and decryption function
  - Unique key set for authentication, encryption and decryption
- 64 Bytes OTP memory
- Embedded application features
  - Support 5 Bytes serial number
  - Support multiple host-client interfaces I2C
  - Wide input power range : 1.8V ~ 3.6V
  - SOT23-6 and 8SOP packages

## 1.2 Application

I2C interface running at 400KHz is used for fast and efficient communications with up to 127 devices that may be individually addressed. The KEROS-Lite is available in industry standard 8-lead or 6-lead packages with the same familiar pin layout.

2 Pin Information

2.1 Application Circuit

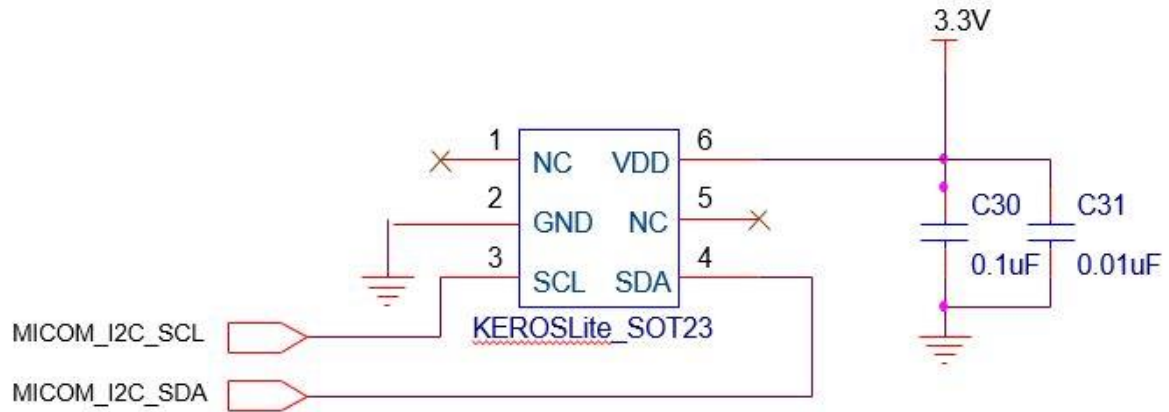


Figure [2.1.1] SOT23-6 Package

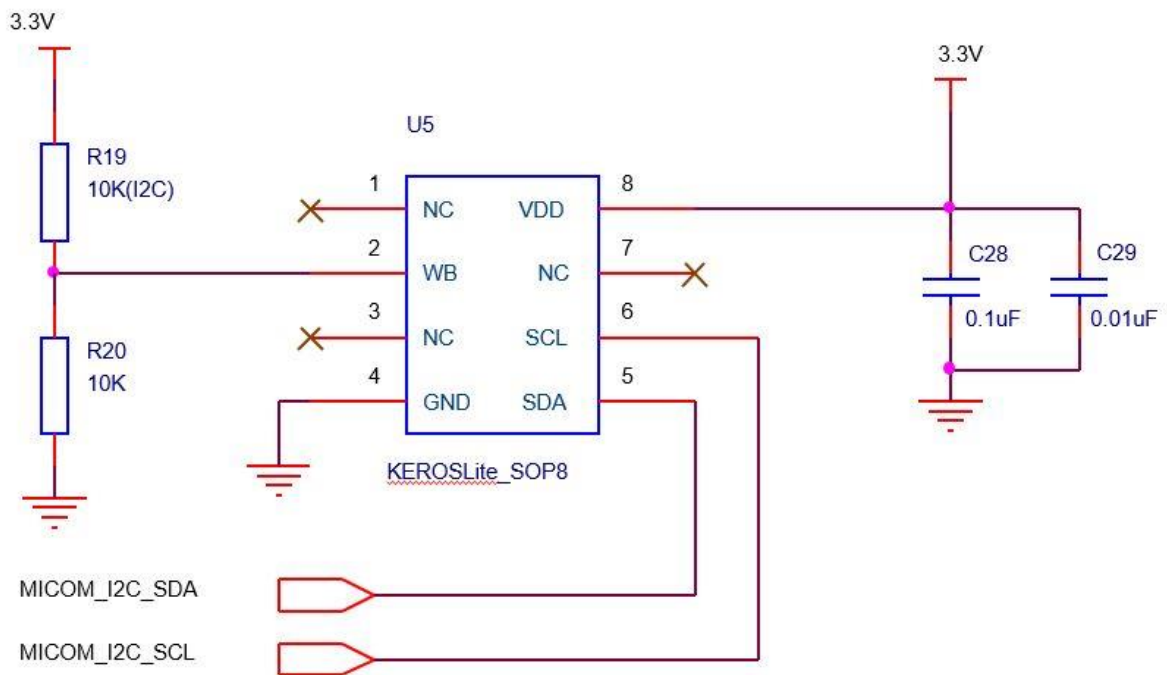


Figure [2.1.2] 8SOP Package

2.2 Pin configuration(SOT23-6)

Pin number	Pin name	Direction	Description
1	NC	-	Not Connect
2	GND	-	Ground
3	SCL	I	Serial Clock
4	SDA	I/O	Serial Data
5	NC	-	Not Connect
6	VCC	-	Power Supply

Table [2.1] SOT23-6 Pin description

2.3 Pin configuration (8SOP)

Pin number	Pin name	Direction	Description
1	NC	-	Not Connect
2	WB	I	Communication Mode Selection High : I2C Low : Not Use
3	NC	-	Not Connect
4	GND	-	Ground
5	SDA	I/O	Serial Data
6	SCL	I	Serial Clock
7	NC	-	Not Connect
8	VCC	-	Power Supply

Table [2.2] 8SOP Pin description

## 2.4 Pin description

### 2.4.1 Supply Voltage (VCC)

The VCC input is 1.8V to 3.6V positive voltage supplied by host

### 2.4.2 SCL

The SCL input used to clock data on the positive clock edge and clock data out on the negative clock edge.

### 2.4.3 SDA

The SDA pin is bi-directional for serial data transfer. This pin is open drain driven and may be wired with any number of other open drain and open collector devices. An external pull up resistor should be connected SDA and VCC, a normal value of 4.7K Ohm may be used. The value of this resistor and the system capacitance loading the SDA bus will determine the rise time of SDA. This rise time will determine the maximum frequency during read operations. Low value pull up resistors will allow higher frequency operations while drawing higher average power supply current.

### 2.4.4 WB

The WB input pin is used for only interface I2C. If WB pin connected to high(VCC), it select the I2C interface. If WB pin connected to low(GND), it is not used.



3 Block Diagram

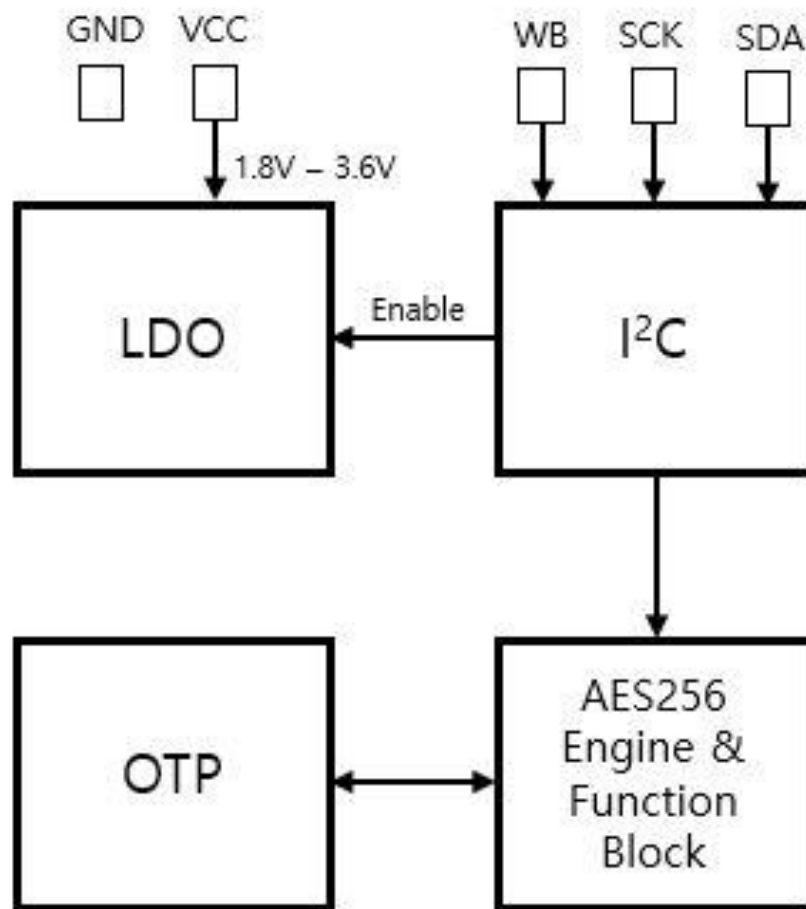


Figure [3.1] KEROS-Lite Block Diagram

4 Operation

4.1 Initial : KEROS-Lite Boot sequence and access wait time

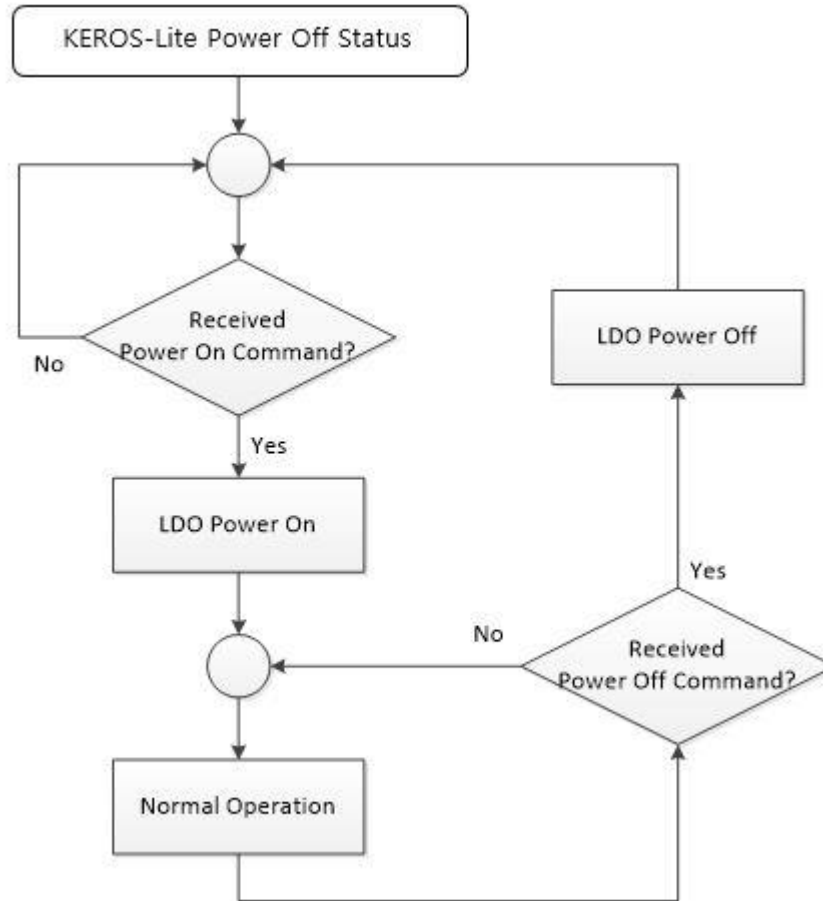


Figure [4.1] Boot sequence flow

The wait time for LDO Power On is about 100us.

4.2 Authentication

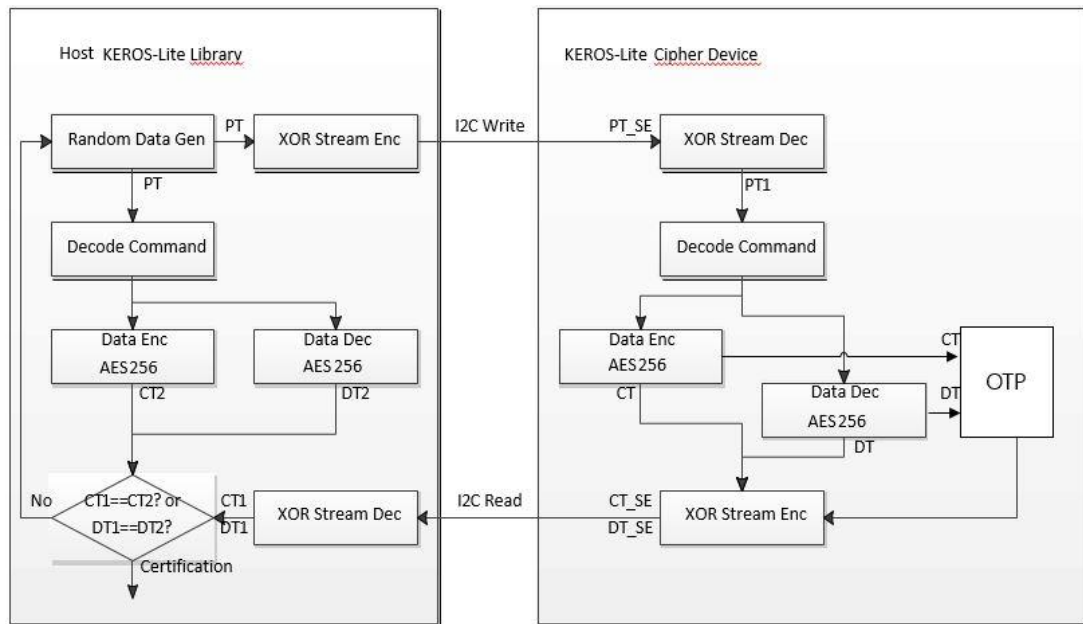


Figure [4.2] Authentication flow

This sequence determines whether the authentication is successful by checking cryptogram which generated by the host and Keros-Lite. If the authentication process of the host is not successful, the authentication of Keros-Lite was failed.

## 5 Communication Protocol

### 5.1 Normal I2C bus type

#### 5.1.1 Write packet

S	Dev Addr	Sub Addr	Data	P
	(1Byte)	(2Bytes)	(nBytes)	

#### 5.1.2 Read packet

S	Dev Addr	Sub Addr	Sr	Dev Addr	Data	P
	(1Byte)	(2Byte)		(1Byte)	(nBytes)	

### 5.2 I2C XOR stream encryption bus type

#### 5.2.1 Write packet

S	Dev Addr	Sub Addr	XOR Index	Data	P
	(1Byte)	(2Bytes)	(1Byte)	(nBytes)(LSB Byte First)	

#### 5.2.2 Read packet

S	Dev Addr	Sub Addr	Sr	Dev Addr	XOR Index	Data	P
	(1Byte)	(2Byte)		(1Byte)	(1Bytes)	(nBytes)(LSB Byte First)	

6 Ordering Part Number

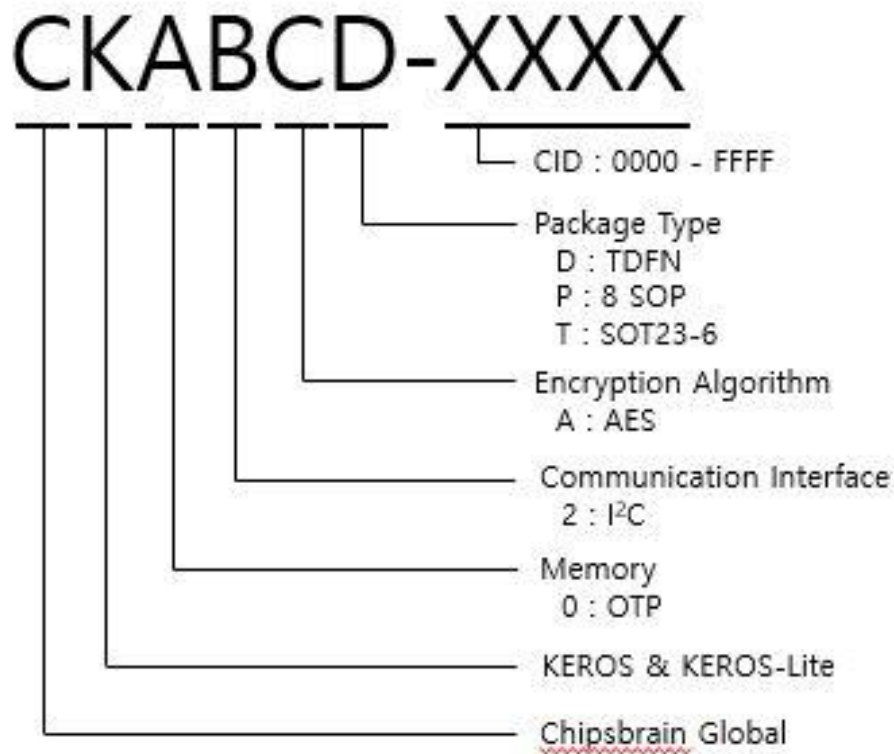


Figure [6.1] Ordering Part Number

7 DC and AC Characteristics

7.1 DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operation Voltage	VCC	Power supply	2.0	3.3	3.6	V
	VDD	Core Power supply(only output)	1.65	1.8	1.95	V
Input Low Voltage	VIL	All input pins	GND-0.3	-	0.3	V
Input High Voltage	VIH	All input pins	VCC-0.3	-	VCC+0.3	
Output High Voltage	VOH	VCC=3.3V IOH=100uA	VCC-0.3	-	-	
Output Low Voltage	VOL	VDD=3.3V IOL=4mA	-	-	0.4V	
Output Low Current	IOL	VOL= 0.4V	-	-	4	mA
Active Power Supply Current	ICC	Normal operation mode VCC=3.3V	-	1.3	3	mA
Sleep Current	ISLEEP	VCC=3.3V		-	1	uA

Table [7.1] DC electrical characteristics

LDO (Ta=25°C, Vcc=3.3V) Characteristics

Parameter	Condition	Min	Typ	Max	Unit	Note
Operating Voltage		2.0	3.3	3.6	V	
Regulation Output Voltage	VCC=2.0~3.6V	1.65	1.8	1.95	V	
Current Drivability	VCC=1.5V	-	-	20	mA	

Table [7.2] LDO characteristics

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	Vdd	-	-0.3 to +3.6	V
Input voltage	Vi	All ports	-0.3 to Vdd+0.3	V
Output voltage	Vo	All output ports	-0.3 to Vdd+0.3	V
Output Current High	Ioh	One I/O pin active	-200	uA
Output Current Low	Iol	One I/O pin active	10	mA
Operating temperature	Ta	-	-20 to +85	°C
Storage temperature	Ts	-	-65 to +150	°C
Junction temperature	Tj		150	°C

Table [7.3] absolute maximum ratings

7.2 AC Parameters

7.2.1 I2C Interface

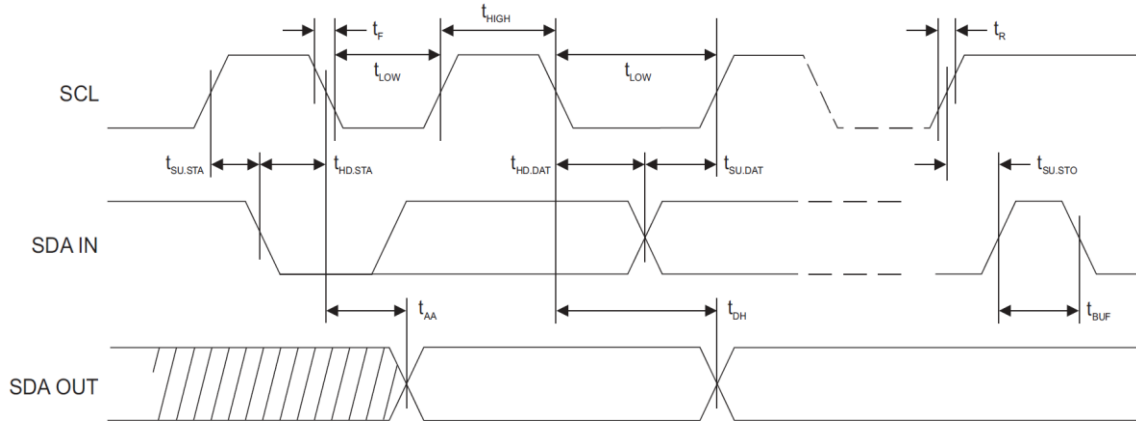


Figure [7.1] I2C interface timing

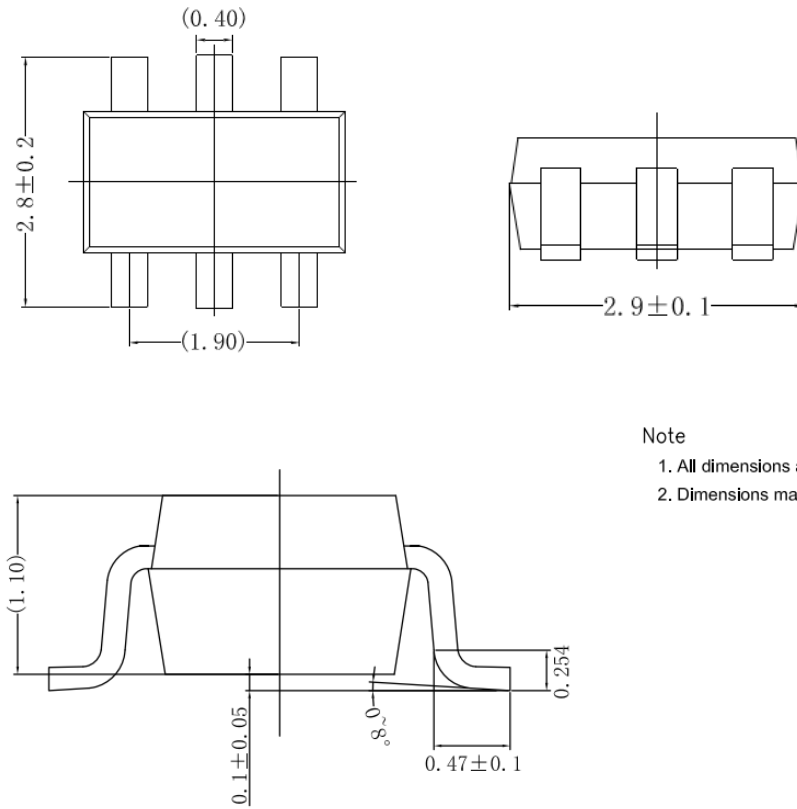
Symbol	Parameter	Min	Max	Units
f <sub>sck</sub>	SCK Clock Frequency	-	400	KHz
	SCK Clock Duty Cycle	40	60	%
t <sub>HIGH</sub>	SCK High Time	1	-	us
t <sub>LOW</sub>	SCK Low Time	800	-	ns
t <sub>SU.STA</sub>	Start Setup Time	500	-	ns
t <sub>HD.STA</sub>	Start Hold Time	500	-	ns
t <sub>SU.STO</sub>	Stop Setup Time	500	-	ns
t <sub>SU.DAT</sub>	Data in Setup Time	100	-	us
t <sub>HD.DAT</sub>	Data in Hold Time	0	-	ns
t <sub>R</sub>	Input rise time	-	300	ns
t <sub>F</sub>	Input Fall Time	-	100	ns
t <sub>AA</sub>	Clock Low to Data Out Valid	100	700	ns
t <sub>DH</sub>	Data Out Hold	100	-	ns
t <sub>BUF</sub>	Time bus must be free before a new transmission can start	1	-	us

Table [7.2] I2C interface parameter



8 Package Dimension

SOT23-6

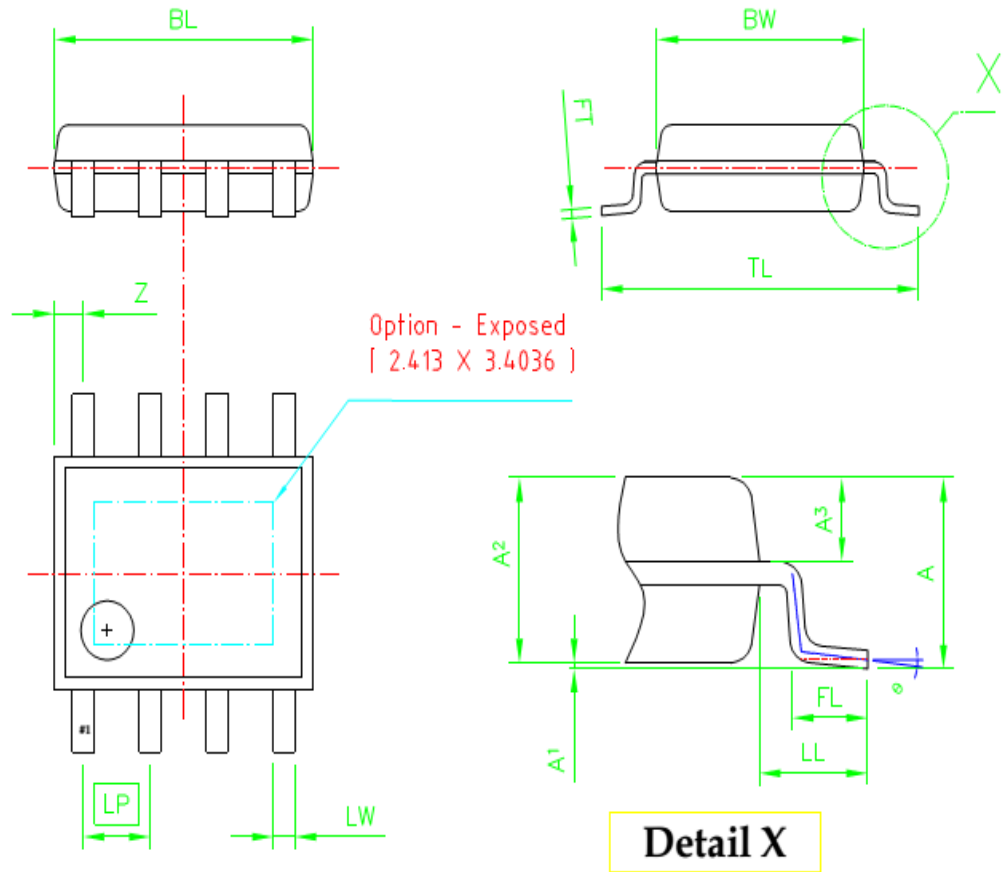


Note

1. All dimensions are in mm
2. Dimensions marked with a parenthesis are reference dimensions

Figure [8.1] package dimension (SOT23-6)

8SOP



### Dimensions

Unit	BL	BW	FT	TL	LP	LW	A <sub>max.</sub>	A1	A2	A3	LL	FL	θ	Z
mm	5.10 4.70	4.10 3.70	0.210 0.196	6.20 5.80	1.27 BSC	0.432 0.381	1.75	0.05 0.25	1.45 BSC	0.623 BSC	1.05 BSC	0.80 0.50	8 0	0.55

Figure [8.2] package dimension (8SOP)