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Intelligent Digital Multi-Mode Flyback Controller HY1602C/D

Revision 1.2

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Intelligent Multi-Mode Flyback Controller

Features

- Intelligent Digital Multi-Mode Control
- Peak Current Mode Control at Burst-Mode /PFM/DCM/CCM
- Continuous-Conduction Mode (CCM) at Low Line(LL), QR at High Line(HL) to Balance the Switching Loss and the Conduction Loss
- Over-load Period up to 56ms
- Switching Frequency Dithering to Improve EMI
- Adaptive MOSFET Gate Drive to Balance Switching Loss and EMI
- MOSFET Gate Voltage is Clamped at 12V
- Meet Limited Power Source (LPS) safety requirements
- Rich Protection Features
 - Output OVP
 - VCC OVP
 - Transformer Saturation Protection
 - Current Sensor Resistor Short Protection
 - Output Over Load Protection
 - On chip OTP
- Line Feed-forward Compensation
- Brown-in and Brown-out
- Power Consumption < 75mW
- Low Start-Up Current (<3 μ A)

Description

HY1602C/D is an intelligent digital multi-mode Flyback controller. The newly developed architecture is inherent features to meet regulatory requirements from around the world.

HY1602C/D integrates rich protections and features such as line compensation, slope compensation, transformer short protection, output over-voltage protection, over-temperature protection, brown in and brown-out, sense resistor short protection.

HY1602C/D has 2 options:

HY1602C: 65kHz, VCC OVP Auto Restart, Output OVP Auto Restart, CV/LPS

HY1602D: 89kHz, VCC OVP Latch, Output OVP latch, CV/LPS

HY1602C/D is available with the SOT23-6 package.

Applications

- Offline Charger
- Programmable travel adapter
- USB PD Charger
- TV / Monitor Standby Power
- Notebook Adapter

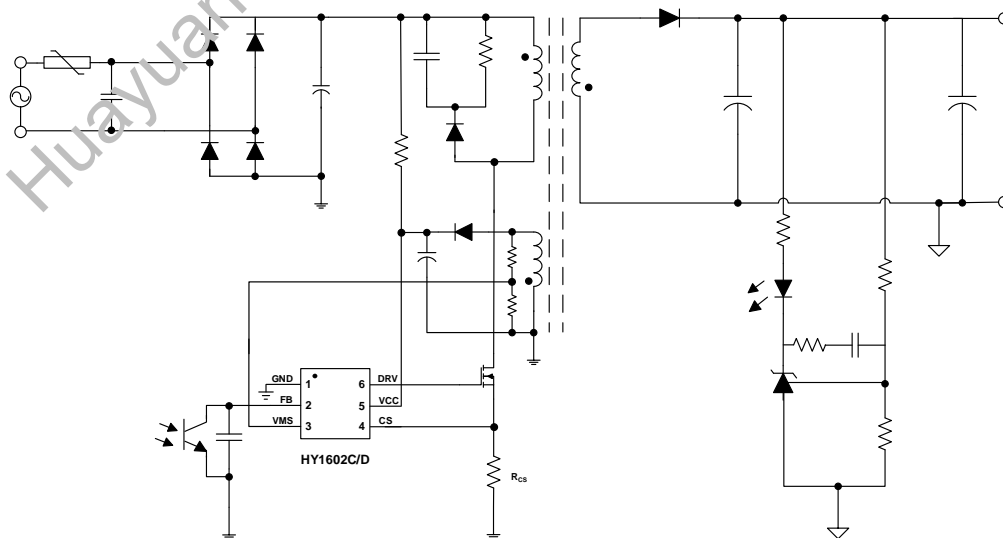


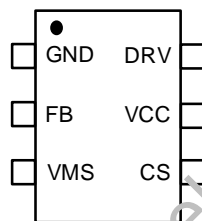
Fig 1. Typical Application Circuit

HY1602C/D Option Table

Product		HY1602C	HY1602D
Switching Frequency	Low Line	65 kHz	89 kHz
	High Line	65 kHz	89 kHz
VCC OVP		Auto Restart	Latch
Output OVP		Auto Restart	Latch

Pin Configuration

(TOP VIEW)



SOT23 6

Functional Pin Definitions

No.	Name	Description
1	GND	Ground.
2	FB	Voltage loop feedback input. Connect an opto-coupler from the FB pin.
3	VMS	Auxiliary winding detection signal input. It detects the input voltage and output voltage information
4	CS	Current sensing input.
5	VCC	VCC is the supply of IC. The controller is enabled when VCC voltage reaches V_{CC_ON} and disabled when VCC drops below V_{CC_UVLO} .
6	DRV	Gate drive output

IC Functional Diagram

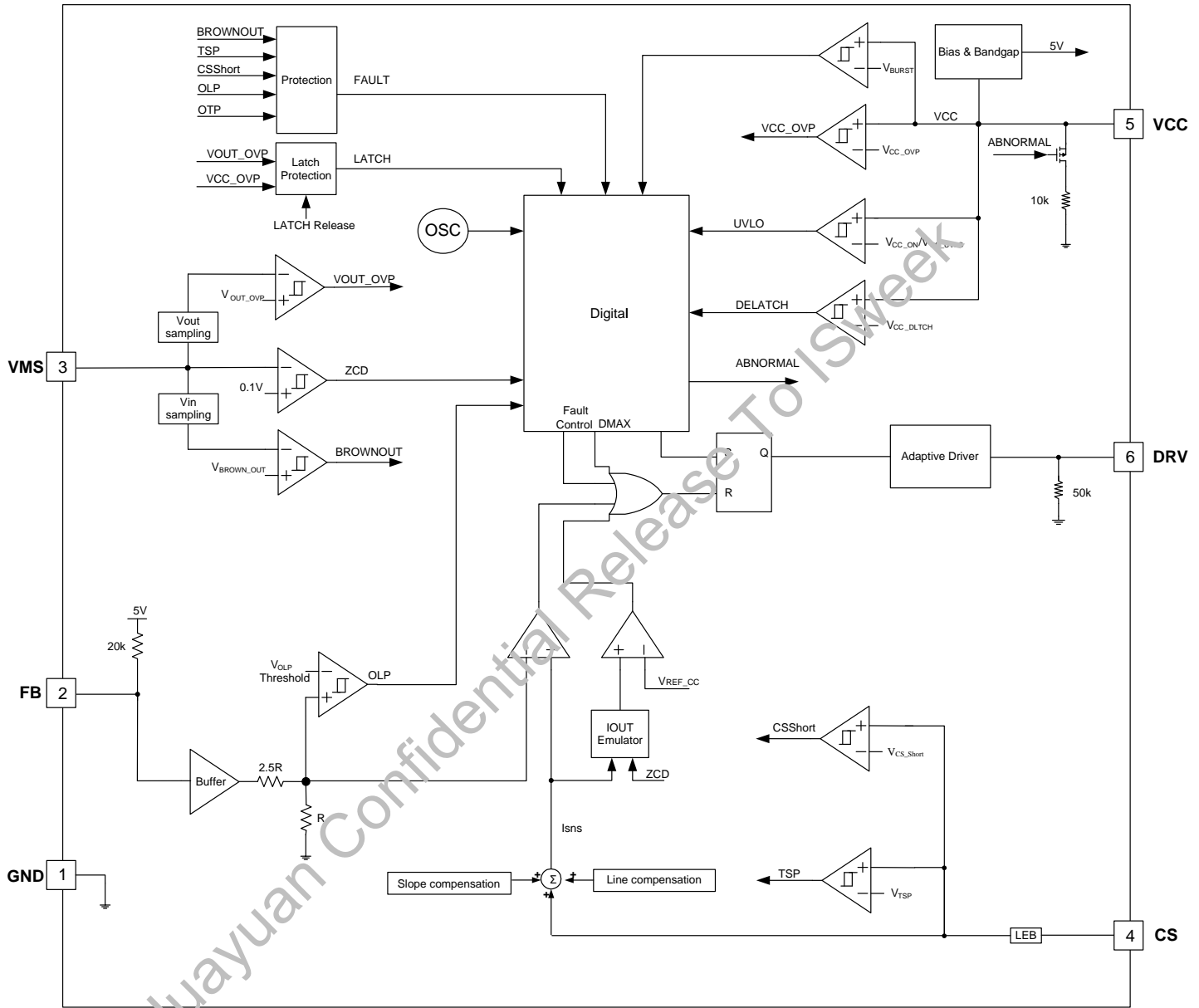


Fig 2. HY1602C/D Simplified Functional Block Diagram

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Min.	Max.	Unit
VCC	VCC	-0.3	40.0	V
DRV	DRV	-0.3	40.0	V
CS, FB, VMS	CS, FB, VMS	-0.3	6.5	V
T _{jt}	Operating junction temperature	-40	150	°C
T _{stg}	Storage temperature	-40	150	°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ESD Ratings

Item	Description	Value	Unit
Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101	±1000	V

Thermal Specification

Item	Value	Unit
R _{θJA} Junction-to-ambient thermal resistance	260	°C/W
R _{θJC(top)} Junction-to-case (top) thermal resistance	135	°C/W

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature T_{J(MAX)}, the junction-to-ambient thermal resistance R_{θJA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_{D(MAX)}=(T_{J(MAX)}- T_A)/R_{θJA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Electrical Characteristics

VCC = 12V, T_{AMB} = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VCC Section						
V _{CC}	Bias Power Supply				39.5	V
V _{CC_OVP}	VCC OVP Threshold		36	38	39.5	V
V _{CC_ON}	Power-On Threshold	V _{CC} Rising	15	16.9	17.5	V
V _{CC_UVLO}	UVLO Threshold	V _{CC} Falling	6.7	7.50	8.3	V
V _{CC_DLTCH}	Delatch Threshold	V _{CC} Falling		4.50		V
I _{CC_NGT}	Quiescent Current	DRV Pin Open			700	μA
I _{CC_WGT}	Operating Current with Load	fs=65kHz, 1nF Load on DRV Pin		2		mA
I _{CC_ST}	Start_up Current	V _{CC} < V _{CC_ON} During Start_up			3	μA
CS Section						
V _{CS_Limit}	Current Limit		0.76	0.80	0.84	V
V _{CS_Short}	Current Sensing Short Threshold		0.06	0.10	0.14	V
V _{TSP_REF}	Transformer Saturation Protection Threshold		1.425	1.50	1.575	V
LEB	Leading Edge Blanking Time			300		ns
V _{REF_CC}	Constant Current Reference		324	360	396	mV
FB Section						
V _{FB}	FB Pin Pull-Up Voltage	FB Pin Open		5.0		V
V _{FB_OLP}	Open Loop Protection Reference		4.0	4.2	4.4	V

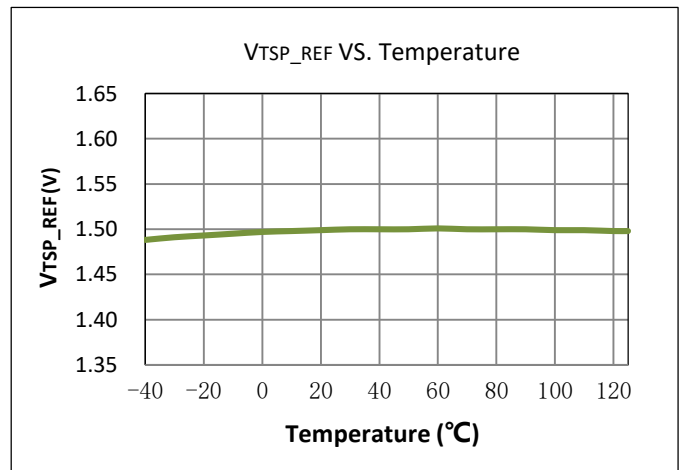
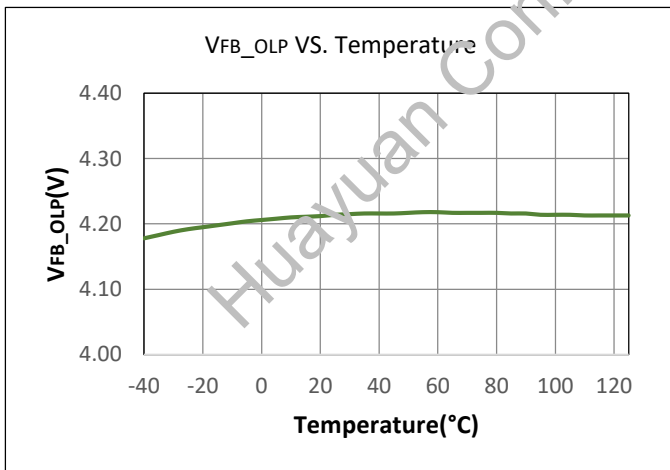
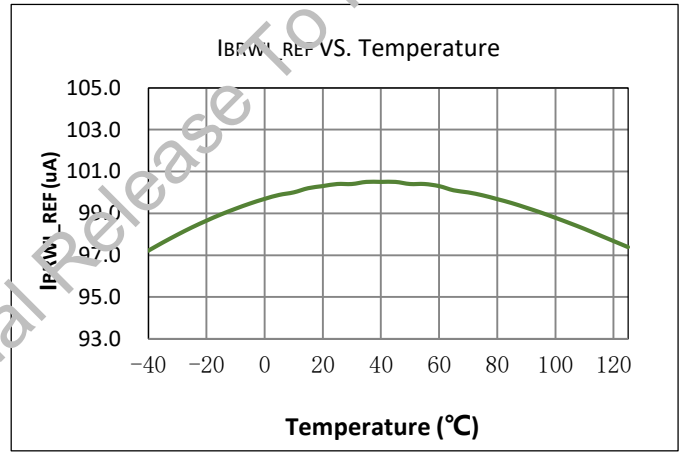
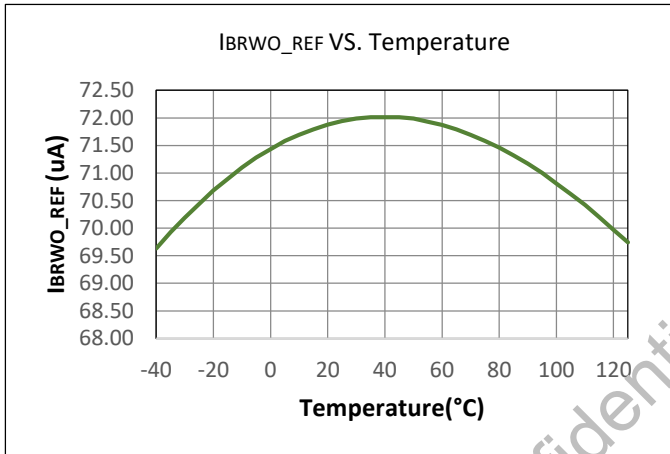
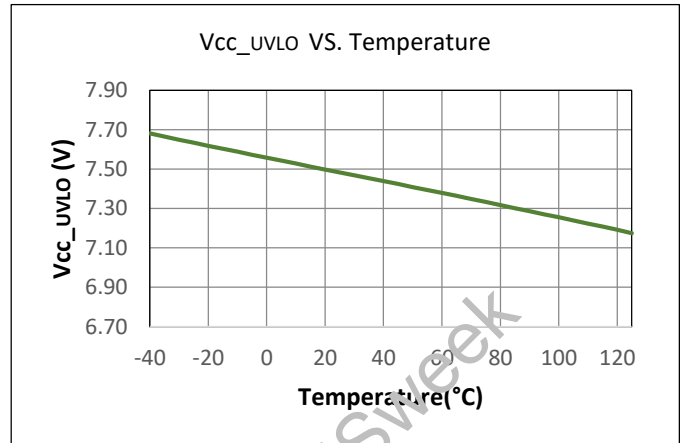
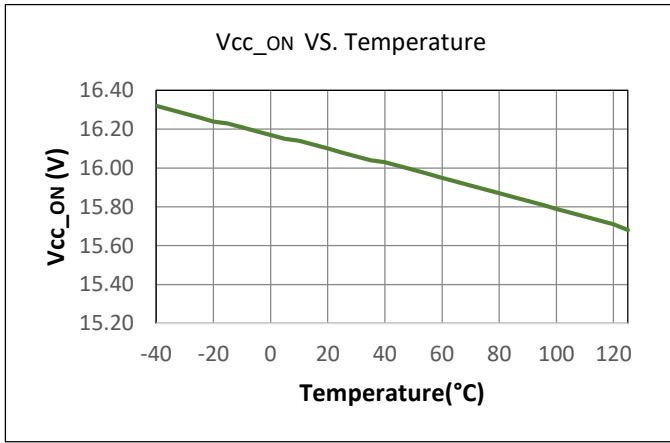
V _{OLP_HYS}	Open Loop Protection Hysteresis			40		mV
V _{BURST}	Burst Mode Entry Threshold		1.15	1.2	1.25	V
V _{BURST_HYS}	Burst Mode Threshold Hysteresis			0.1		V
R _{FB}	FB Pin Pull_up Resistance		14	20	26	kΩ
VMS Section						
V _{SNS}	Maximum Voltage				5.5	V
V _{OUT_OVP}	Output Voltage OVP Reference		2.35	2.5	2.65	V
I _{BRWO_REF}	Input Line Voltage Brown Out Reference			72		μA
I _{BRWI_REF}	Input Line Voltage Brown In Reference			100		μA
I _{HLL_LL}	High/Low Line Detection Reference			218		μA
T _{Vsns_blk}	Vsns blanking time	V _{FB} > 1.75V		2.5		μs
		V _{FB} < 1.5V		1.4		μs
DRV Section *						
V _{DRV_CLP}	DRV Clamped Voltage			12		V
R _{ON_PUP}	Pull_up R _{DS_ON}			180		Ω
R _{ON_PDW}	Pull_down R _{DS_ON}			26		Ω
T _{RISE}	Output Rising Time, 10% to 90%	C _L =1nF		200	300	ns
T _{FALL}	Output Falling Time, 90% to 10%	C _L =1nF		50	100	ns

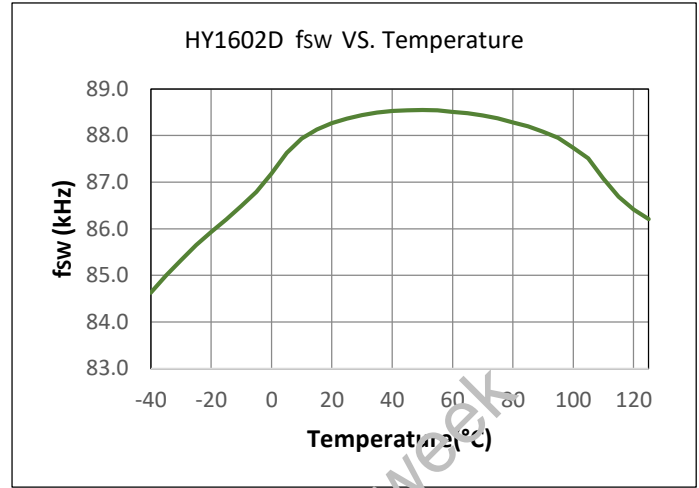
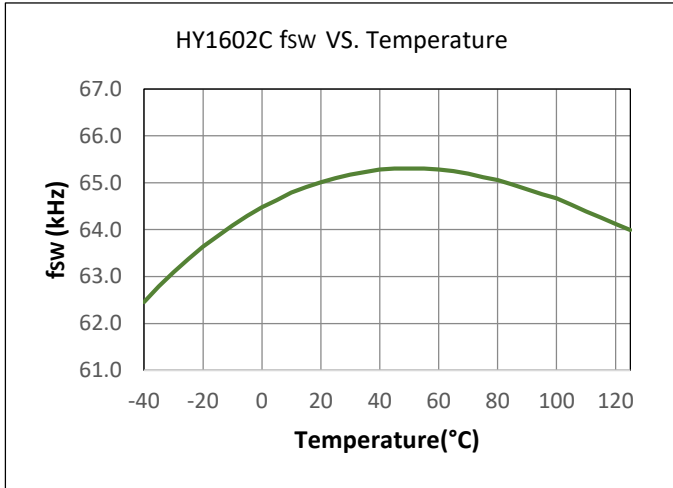
T _{ON_MIN}	Minimum PWM ON			600		ns
T _{OFF_MIN}	Minimum PWM OFF			2.6		μs
PWM Section						
f _{sw}	Base Switching Frequency	HY1602C	60	65	70	kHz
		HY1602D	82	89	96	kHz
Δf	Frequency Jittering Range			±5%		
OTP Section						
T _{OTP}	Over Temp Protection	(Note 3)	140			℃
T _{OTP_Hys}	OTP Hysteresis	(Note 3)		50		℃

Note 3. Guaranteed by design.

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Typical Characteristics





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Detailed Function Description

HY1602C/D is a high performance, high integration, secondary side feedback AC/DC Flyback PWM controller. It implements the advanced digital control scheme to achieve high efficiency, better EMI and high performance at low total system cost. HY1602C/D operates at Quasi-Resonant (QR) mode under high line. It operates CCM under low line condition in order to improve efficiency and reduce bulk capacitance.

Multi-Mode

HY1602C/D is a digital multi-mode PWM controller. It operates Burst/PWM/PFM/QR/DCM/CCM control alternately based on the line input voltage, feedback voltage, as shown in Fig 3 and Fig 4. Under high line condition, it operates at QR mode. Under low line condition, it operates at CCM with switching frequency at 65/89kHz. As the load decreases, it enters into DCM operation. The switching frequency is decreased from 65/89 kHz to 25 kHz following the frequency profile. At light load, the controller operates at the burst mode.

The high line or low line input can be determined by the HL/LL threshold on VMS. The maximum switching frequency at the high line is fixed at 65/89kHz. The low line mode can operate CCM mode with 65/89kHz.

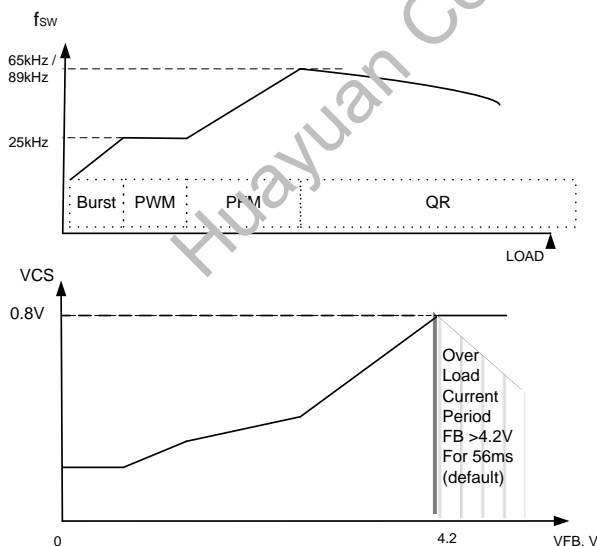


Fig 3. High Line Load Profile

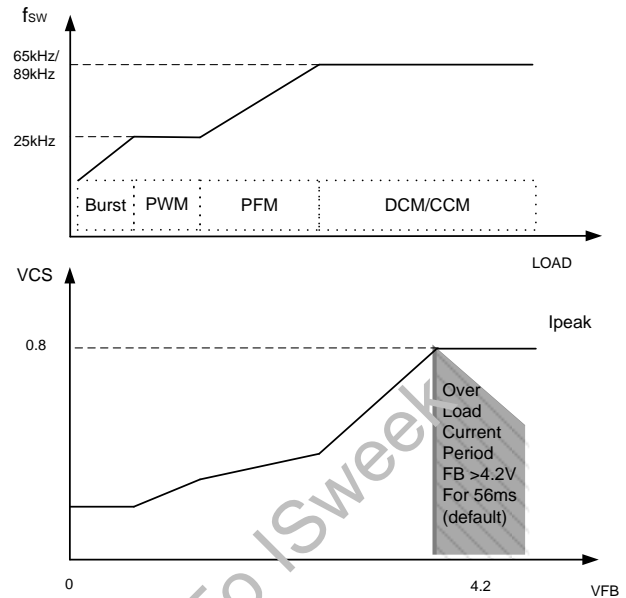


Fig 4. Low Line Load Profile

Start-up

The start-up time specification of adapter is generally less than 3 seconds. The VCC voltage of the HY1602C/D generated from start-up resistors and the bias winding after start-up. HY1602C/D consumes less than 3μA current (ICC_ST) till VCC reaches the threshold of VCC_ON. It enables all internal block bias based on power sequence and MOSFET driver. As the output voltage is ramping up, the bias winding voltage is going up accordingly. The VCC voltage is going down from VCC_ON once the normal operation begins till the bias voltage takes over to charge the VCC capacitor.

Soft Start

After VCC reaches VCC_ON threshold, HY1602C/D begins the soft start.

The HY1602C/D soft start threshold and timing is show in Fig 5.

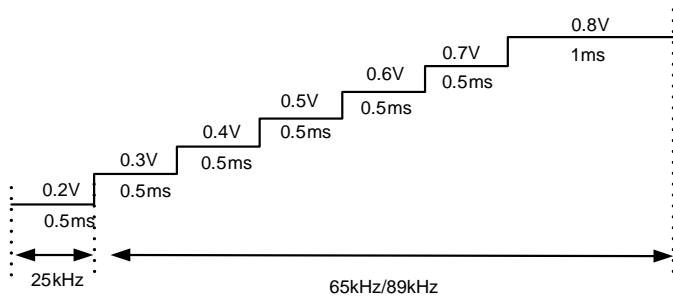


Fig 5. Soft-Start with 4ms Timing and Threshold

In HY1602C/D, the soft start is implemented as a predetermined peak current control within 4ms. For first 0.5ms, the switching frequency is 25kHz and the predetermined peak current control voltage command across sensing resistor is 0.2V in order to achieve the transformer demagnetizing. The next level is the peak current control voltage as 0.3V for 0.5ms under 65/89kHz switching frequency. The following peak current control voltage step is increasing 0.1V for every 0.5ms to 0.8V following the incremental pattern. The duration of 0.8V step is 1ms instead of 0.5ms. During the soft start, the feedback voltage and the peak current control are decoupling. The soft start will be terminated once the feedback voltage is lower than the predetermined peak current level.

Line Compensation

HY1602C/D implements the line compensation scheme to add the offset voltage on CS pin in order to compensate the propagation delay which is caused by the turn-off delay. This line feedforward compensation is able to maintain the same output power under all range of input voltage condition.

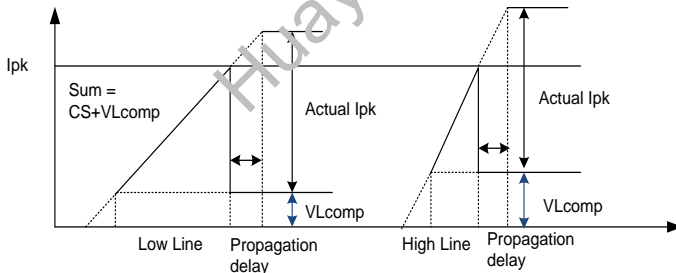


Fig 6. Line Compensation

HY1602C/D indirectly senses the input line. When the MOSFET is on, the bias winding has a negative voltage by the primary to bias winding ratio. The current on the VMS is calculated by VMS voltage divided by R_{UP} Resistor. The internal current source corresponds to the DC bulk voltage through the bias winding.

$$I_{VIN} = \frac{N_B}{N_P} \cdot \frac{V_{BULK}}{R_{UP}}$$

Limited Power Source (LPS)

Power supply designed for 20V/3A may generally delivery current of 12A when output is down to 5V, under keeping constant output power operation. Thus, violate the Limited Power Source (LPS) safety requirements for the maximum output current, and may damage its connected devices. In order to achieve reliable operation, HY1602C/D employs innovative schemes to measure output current without directly sensing output current.

In DCM flyback converter, the output average current, I_o ,

$$I_o = \frac{1}{2} \cdot N \cdot \frac{V_{CS}}{R_{CS}} \cdot \frac{T_{rst}}{T_p}$$

Define an internal CC reference voltage of V_{REF_CC} as the constant value and can be used to determine the maximum output current.

$$V_{REF_CC} = I_{out} \cdot \frac{R_{CS}}{N}$$

Protections

HY1602C/D achieves various protections as listed in below table, including VCC OVP, Output OVP, RCS Short Protection, Transformer-Short Protection (TSP), Over Load Protection (OLP), Over-Temperature Protection (OTP), Brown-Out/in Protection.

Protection	Response
VCC OVP	HY1602C: Auto restart
	HY1602D: Latch
Output OVP	HY1602C: Auto restart
	HY1602D: Latch
R _{CS} Short Protection	Auto restart
Transformer Saturation Protection TSP	Auto restart
Over Load Protection	Auto restart
On Chip OTP	Auto restart
Brown Out/In	Auto restart

VCC OVP

When VCC pin voltage reaches threshold, V_{CC_OVP}, HY1602C/D performs VCC OVP protection function. For HY1602C, VCC_OVP is an auto restart type protection. For HY1602D, VCC_OVP is latch type protection and de-latched after AC recycle when V_{CC} voltage is discharged below V_{CC_DLTCH}.

Output OVP Protection

The output voltage is sensed from the auxiliary winding on the VMS pin. The voltage level is detected from the rising edge of VMS after debounce time. The voltage level is compared with the OVP threshold (V_{OUT_OVP}). If the voltage level is above the OVP threshold, HY1602C shuts down the gate signal

and enters into auto restart mode. Under auto restart mode, HY1602C gate signal recovers once the OVP threshold is not triggered. Different from HY1602C, HY1602D shuts down the gate signal and enters into latch mode. This latch is released with AC power off and V_{CC} voltage is discharged below V_{CC_DLTCH}.

Rcs Short Protection

If R_{CS} is shorted, the system might damage. To prevent the damage, HY1602C/D implements the scheme to detects R_{CS} short and shut down the PWM.

Transformer Saturation Protection (TSP)

TSP is performed when there is a transformer saturation. It could happen when both secondary rectifier and primary MOSFET turns on overlap. It is implemented through the comparator with V_{TSP_REF} threshold. The current slew rate is very high under the transformer saturation as only leakage inductance limits the transformer current rate. If current sensing voltage signal triggers TSP threshold after LEB. IC performs TSP to shut down the PWM signal once the TSP threshold is triggered, HY1602C/D keeps as off state till next power reset event.

Over Load Protection (OLP)

The maximum current sense voltage is limited at V_{CS_LIMIT}. When the current sense voltage reaches at V_{CS_LIMIT}, and the switching frequency also reaches the f_{SW_PK}, the maximum output power is limited. If the output load keeps increasing, the output voltage keeps dropping, then the feedback voltage V_{FB} keeps increasing, when the V_{FB} reaches the V_{FB_OLP} (4.2V typical), HY1602C/D counts from 56ms and then shuts down. The OLP function is enable after the soft-start.

When the feedback circuit such as opto-coupler opens, V_{FB} pin is also pulled up to V_{FB_OLP}, HY1602C/D also shuts down after 56ms.

Over Temperature Protection (OTP)

The internal die temperature is sensed to prevent from over-heat. The temperature reference for OTP is defined at 145 °C typical with 50 °C hysteresis. When OTP fault signal is detected, the OTP is activated to shut down PWM. HY1602C/D try to power-up until the die temperature drops down to 95 °C.

Brown Out and Brown In

HY1602C/D detects brown out and brown in condition through the current output from VMS pin under normal operation. When the current from VMS pin to the bias winding through the bias winding top resistor is below I_{BRWO_REF} , the brown out condition triggers. The PWM is shut down after debounce time once brown out condition triggers. When the current from VMS pin to the bias winding through the bias

The typical bottom resistor value is calculated based on V_{BRWO} as:

$$R_{DW} = \frac{V_{OUT_OVP_REF} \times V_{BRWO} \times \frac{N_B}{N_P} - 0.15 \times (V_{OUT_OVP} \times \frac{N_B}{N_S} - V_{OUT_OVP_REF})}{I_{BRWI_REF} \times (V_{OUT_OVP} \times \frac{N_B}{N_S} - V_{OUT_OVP_REF})}$$

Where, V_{BRWO} is the brown out voltage on the bus after the bridge, V_{OUT_OVP} is the output OVP voltage, N_B is the bias winding turn number, N_P is the primary

winding top resistor is above I_{BRWI_REF} , the brown in condition triggers.

Bias winding resistor divider circuit is used to detect output voltage, input voltage brown out/brown in and high line/low line conditions, as shown in 0.

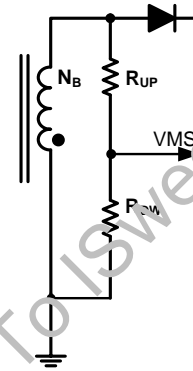


Fig. 1. Bias Winding Detection Circuit

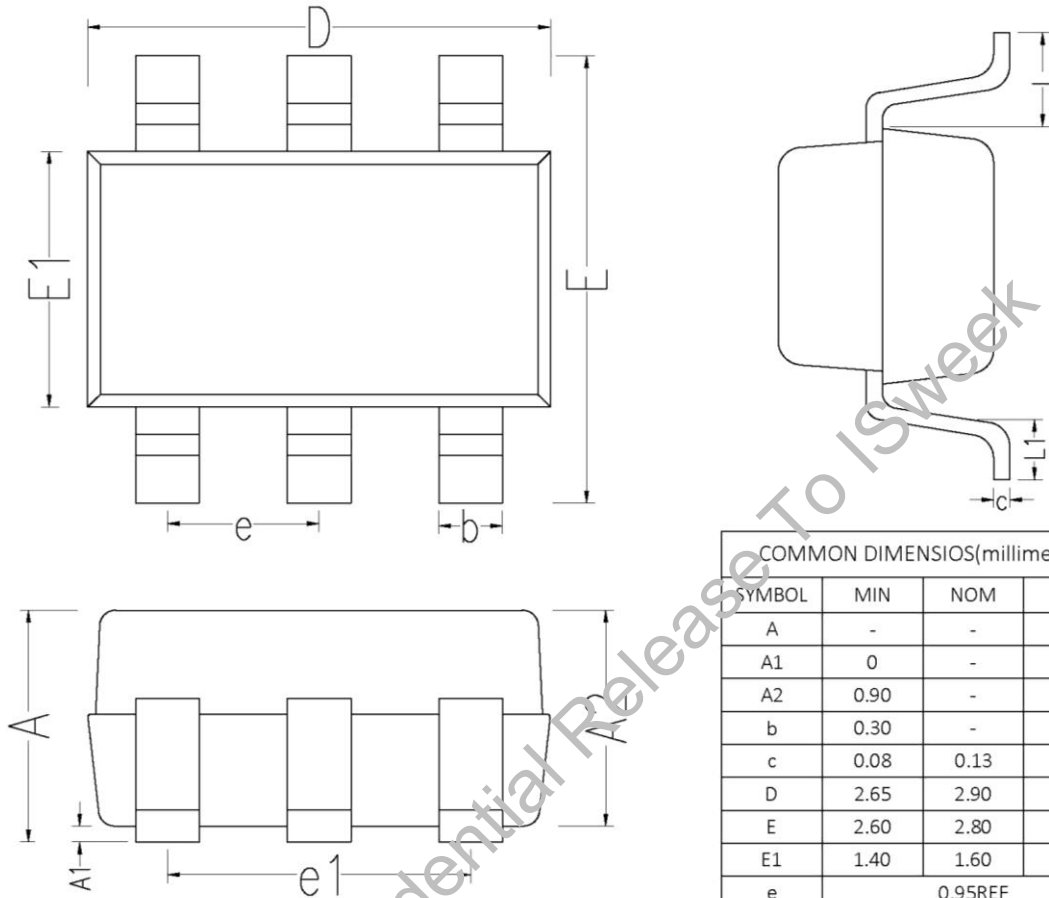
side turn number, N_S is the secondary side winding turn number.

The typical top resistor value is calculated as:

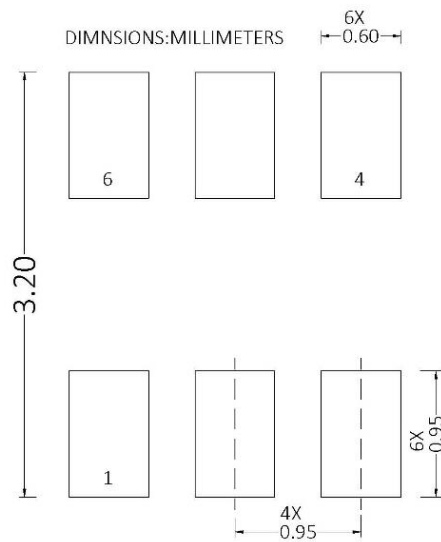
$$R_{UP} = \frac{V_{BRWO} \times \frac{N_B}{N_P}}{I_{BRWI_REF} + \frac{0.15}{R_{DW}}}$$

In the practical design, the resistor of the divider is round to the closest standard resistance value.

SOT23-6 Package

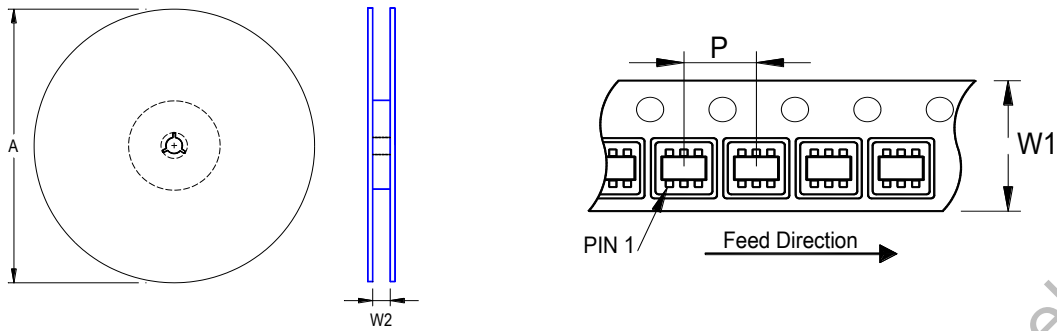


COMMON DIMENSIOS(millimeter)			
SYMBOL	MIN	NOM	MAX
A	-	-	1.45
A1	0	-	0.15
A2	0.90	-	1.30
b	0.30	-	0.50
c	0.08	0.13	0.20
D	2.65	2.90	3.15
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95REF		
e1	1.90REF		
L	0.50	0.60	0.70
L1	0.30	0.45	0.60



Recommended Land Pattern

Tape and Reel Information



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Q'ty Per Reel pcs	Reel Width (W2) Min./Max. (mm)
			mm	inch		
SOT23-6	8	4	180	7	3000	8.4/9.9

Packing Information

Item	Package	Pcs/reel	Reel/Reel box	Reel Box Size (mm)	Reel box/Carton Box	Carton Box Size(mm)	Pcs/carton Box
1	SOT23-6	3000	10	210*210*210	4	445*445*230	120000

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